Advanced
Micro
Devices

ISDN Systems Engineering Application Notes

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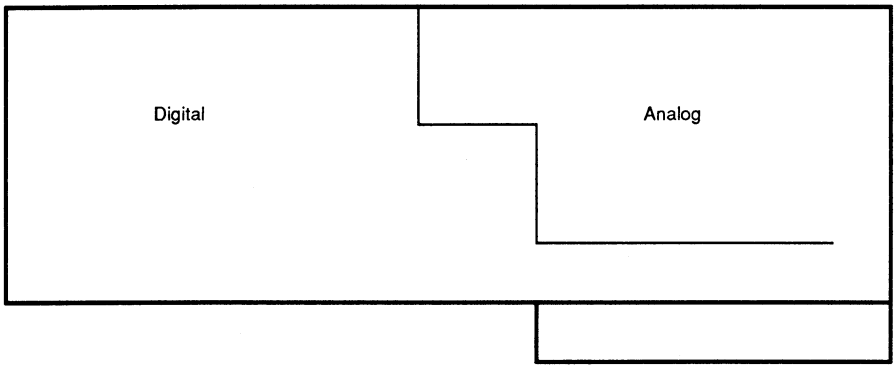
Am79C30A DSC Layout Hints

The Am79C30A integrates high-speed digital logic and sensitive audio circuitry into a single device. Although audio transmission tests are demanding, observance of basic guidelines of component selection and layout will yield excellent performance.

SEPARATE ANALOG AND DIGITAL AREAS

In the example below, a card containing digital circuitry as well as a Digital Subscriber Controller (DSC) has been designed for use in a PC. Four Printed Circuit Board (PCB) layers are used: two for signals and the other two for power and ground. The Vcc and Vss planes of the PCB include cuts which separate the board into two areas that are joined near the edge connector. The DSC and all analog circuits are placed on the right side of the power-plane cuts, as close as possible to the S interface and telephone connectors on the card edge. Since DSC analog and digital functions are manufactured on a single substrate, it is necessary to use a common power supply for the analog and digital Vcc pins of the DSC PLCC to avoid the possibility of excessive current flow through the DSC. The power-plane cuts illustrated in the diagram below reduce the coupling of digital switching noise into the supply path of the DSC and analog components.



UTILIZE EFFECTIVE DECOUPLING PRACTICES

Capacitor selection—For an application such as the one on the previous page, it is recommended to use 0.1-µF high-frequency ceramic capacitors on each IC, and in parallel with 10.0-µF tantalum capacitors near the edge connector. It is important to check for special decoupling requirements for individual ICs, since some functions (for example, dynamic RAM controllers) require bulk decoupling near the package to handle sudden switching loads. For the DSC, it is necessary to include bulk decoupling capacitors if the loudspeaker outputs drive a heavy current load.

Capacitor placement—Individual decoupling capacitors should be placed as close as possible to the supply pins of the IC, with minimum lead length. This is because at higher frequencies the inductances of the capacitor and IC leads are not negligible, and sudden surges of supply current will result in noise spikes on the supply pins.

Decouple all supply pins—On devices such as the DSC in a PLCC package, it is helpful to provide decoupling for each supply pin. Analog Vcc should be decoupled to Analog Vss, and Digital Vcc to Digital Vss, using high-frequency 0.1-µF ceramic capacitors.

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PLAN AN EFFECTIVE BOARD LAYOUT

Care in routing—In an analog environment, it is particularly important to keep signal traces as short as possible, and to route analog traces away from high-frequency signals such as clock lines. Traces that are connected to ground may be used to help isolate key signals. The longer a trace becomes, the greater will be its tendency to act like an antenna or transmission line. It is well worth the time to plan the location of components to minimize the length of critical traces. For example, if a low-level signal to be amplified enters a board through a connector, it is preferable to place the amplifier as close as possible to the connector itself. Although the noise floor may be low, any noise picked up would be amplified along with the signal.

Care in placement—The overall noise performance of a board is also improved by taking precautions in the placement of components. For all devices with crystal oscillators, it is recommended to place the crystal and load capacitors as close as possible to the crystal pins of the device. For the DSC, it is also helpful to place the RC network for the Main Audio Processor (MAP) as close as possible to the DSC CAP1 and CAP2 pins to reduce the coupling of noise into the device.

CCITT I.430 Tutorial

CCITT Recommendation I.430 defines the Layer 1 characteristics of the user-network interfaces at the ISDN S and T reference points. The Am79C30A Digital Subscriber Controller is fully compliant with I.430, and it is instructive to examine I.430 in detail to understand its implications in both IC and system design.

INTRODUCTION: THE ROLE OF I.430

It is important to note that although CCITT Recommendation I.430 is an international specification, the requirements for network connection vary from country to country and are still under development. It is unlikely that a single comprehensive international specification will evolve in the near future; a more likely scenario is that individual countries will at first adopt their own extensions of I.430. For example, in the United States the American National Standards Institute (ANSI) is developing a standard that basically conforms with I.430, but also "specifies individual departures from CCITT I.430 that reflect the domestic environment of the United States." These departures are numerous, including for example differences in power feeding, hazardous voltage protection, and use of the multiframing bits. These differences are in general extensions to or clarification of I.430, as opposed to being incompatibilities. The creation of a single world standard is of necessity a slow process, and it is inevitable that there will be such temporary differences as we converge towards a true global network.

An additional factor in the ISDN environment is certification with individual switch vendors. In the world of analog networks, a telephone or modem device would be tested for compliancy with the specifications of the governing telecommunications authorities (for example, FCC Part 68 in the United States) whereupon the device could be connected to the analog network. In the ISDN environment, switch vendors have independently developed products while the specifications evolved, resulting in the need to undergo compliancy tests with each individual switch vendor for the physical, link, and signaling layers. Fortunately, these specifications are generally equivalent to or slightly relaxed from I.430 at the physical layer, with the majority of differences occurring in signaling. An example of such a specification is AT&T 5D5-900-301.

CCITT Recommendation I.430 is thus seen to be a basic document for the development of equipment for the ISDN S and T reference points, but for the foreseeable future designers will need to look to telecommunications regulatory agencies and ISDN switch vendors for additional requirements.

GENERAL OVERVIEW

Sections 1 and 2 of I.430 present a general description of the reference configurations applicable to I.430, and an overview of the services to be provided to Layer 2 and the management entity (ME). Layer 2 refers to the next higher layer of the OSI software model, which is responsible for certain physical link functions. The ME services all OSI layers with a wide range of system functions, including event notification, error handling, maintenance loops, memory management, and initialization. It is important to note that there is currently no finalized international standard for the functions of the ME or its interfaces to the various OSI layers. Work is underway on a series of CCITT Recommendations (Q.940, 941, 942) in an attempt to standardize ME functions and interfaces; however, at the current time, designers are implementing unique and potentially incompatible versions. Of particular interest in Section 2 are the primitives to be passed between Layer 1 and other entities. For instance, Layer 2 or the ME. I.430 specifically states that these primitives represent the logical exchange of information and control, and are not intended to constrain the implementation of entities or interfaces. No assumption is made about the definition of the other layers or entities to which I.430 is to be connected. For instance, I.430 defines activation/deactivation primitives to be passed between Layers 1 and 2, yet the Q.921 Layer 2 specification makes no mention of what to do with these primitives. The point to be understood here is that I.430 does not specify a software interface, either to the management entity or to Layer 2.

MODES AND CONFIGURATIONS

Sections 3, 4, and 8 of I.430, together with Annex A, describe the modes of operation and wiring configurations of the user-network interface. In "point-to-point" operation a single TE and a single NT are interconnected, whereas in point-to-multipoint operation multiple TEs may be simultaneously connected to a single NT in either a "short passive" or "extended passive" bus configuration. The timing recovery requirements for the NT side vary in the different wiring configurations, and I.430 defines four classes of NT that operate on some or all of the three wiring configurations. NTs may be designed

for short passive bus operation only, for both point-to-point and passive bus, for extended passive bus only, or for point-to-point only.

In the short passive bus wiring configuration, up to eight TEs may be connected at random points along the cable. If the NT device uses fixed timing, it samples data at regular fixed intervals even though pulses arrive from the various terminals with different transmission delays. This implies that the maximum time difference between pulses arriving at the NT must be less than a bit period. The round-trip delay for NTs configured for passive bus only operation may vary from 10 to 14 microseconds, the lower value of 10 microseconds being derived from the 2-bit delay through the TE plus the maximum negative phase deviation. With fixed timing, it is the round-trip delay that limits the maximum cable length of the short passive bus configuration and not the attenuation of the cable itself. This delay corresponds to a maximum distance on the order of 100–200 meters for the short passive bus configuration.

The simplest configuration is point-to-point, where a TE is present at one end of the cable and an NT at the other. In this case, the maximum transmission distance is determined by cable attenuation and receiver performance, not round-trip delay. The accepted target distance for point-to-point operation is 1 kilometer. Adaptive NT timing is required, which uses a phase-lock loop to compensate for the round-trip delay. NTs that are configured for point-to-point operation only must accommodate round-trip delays, which may vary from 10 to 42 microseconds. NTs that are configured for either point-to-point or short passive bus operation must allow delays ranging from 10 to 42 microseconds for point-to-point, and 10 to 13 microseconds for short passive bus.

In the extended passive bus configuration, the maximum cable distance is increased over the short passive bus by grouping the terminals together at the far end of the cable, thereby restricting the range of the differential round-trip delay between any two terminals. In this case the NT again uses adaptive timing. Although the calculations in Annex 4 indicate up to four TEs in this configuration, it is left up to individual regulatory authorities to define detailed configurations. The distance objective of the extended passive bus configuration is 1 kilometer, but will vary greatly with the wiring of the TEs. NTs configured for extended passive bus operation only must accommodate round-trip delays ranging from 10 to 42 microseconds.

Note that in all three configurations there is only one terminating resistor at each end of the cable, regardless of the number of terminals connected. The presence of extra terminating resistors will artificially degrade distance performance.

The final diagram of Annex A shows a star configuration NT1, in which point-to-multipoint operation is realized using point-to-point wiring. In this case, the NT1 must do extra buffering and processing of the D-channel echo bits to handle contention by all the TEs for the single D channel on the network side of the NT1.

An interesting point in Section 4 is that the correct polarity of wiring must be maintained in the TE to NT direction for point-to-multipoint configurations. This is because all D-channel MARKs must appear as LOW MARKs to ensure proper operation of the D-channel priority mechanism.

FUNCTIONAL CHARACTERISTICS

Section 5 of I.430 summarizes the basic functions of an I.430-compatible interface.

Two B Channels each provide a 64-kb/s full-duplex channel for user information. No restriction on the content or usage of these channels is defined, other than the requirement that they do not contain circuit switching information for the network.

Bit timing recovery from the data stream is necessary since the four-wire interface does not provide any separate data clocks.

Octet timing provides the TE and NT with an 8-kHz frame-sync signal.

Frame alignment allows the TE and NT to correctly identify and recover the time division multiplexed overhead bits and data channels.

The D channel provides a 16-kb/s full-duplex channel for user data packets and network signaling packets.

Power feeding is included as an I.430 function, but implementations and requirements vary greatly depending upon the regulatory environment.

Deactivation and activation are procedures defined to direct the TE and NT into or out of low-power idle states.

Connection and disconnection of a TE at the interface is defined as the appearance and disappearance respectively of power to the TE. These events are significant in the higher-level procedures that assign a unique TEI (Terminal Endpoint Identifier) number to each TE during system initialization.

The formats of the 48-bit frames are then defined, which are different for each direction of transmission. Figure 3 of I.430 is appended to the end of this application note for reference.

FRAME STRUCTURE AND ALIGNMENT

In the I.430 pseudo-ternary line code, a binary ONE (SPACE) is represented by no line signal, whereas a binary ZERO (MARK) is represented by either a positive or negative pulse. Transmitted binary ZEROs must alternate in polarity to maintain "DC balance" on the line,

with the exception of intentional "code violations" in the frame where successive ZEROs do not alternate in polarity.

Both types of frames begin with a framing bit F, which is always a positive MARK, followed by a balance bit L, which is always a negative MARK. The last MARK of the previous frame is guaranteed to be positive, meaning that the F bit is a code violation. The first MARK following the frame balance bit is required to be a negative MARK, which produces a second code violation. In the NT to TE direction, the auxiliary framing bit F_A or the N bit guarantee the required violation within 14 bits or less from the F bit if the data bits between L and F_A do not. If the multiframing mode (to be discussed in detail shortly) is enabled, the NT will transmit a SPACE in the F_A position and N will be a MARK. If multiframing is not enabled, the NT will send a MARK in the F_A position and N will be a SPACE.

In the TE to NT direction, the F_A bit will guarantee a second code violation within 13 bits or less from the F bit if multiframing is not enabled. If multiframing is enabled, only 4 out of 5 frames are guaranteed to satisfy the 13 or less criterion, but the framing procedures are tolerant of this missing violation.

In the NT to TE direction, frame synchronization is achieved when 3 consecutive frames with valid pairs of code violations satisfying the 14-bit criterion are detected. Loss of synchronization occurs when a period of time equivalent to 2 consecutive frames elapses without detection of violations that satisfy the 14-bit criterion, whereupon the TE must cease transmission immediately.

In the TE to NT direction, frame synchronization is achieved when 3 consecutive frames with valid pairs of code violations satisfying the 13-bit criterion are detected. If all F_A bits are ZERO, loss of synchronization occurs when a period of time equivalent to 2 consecutive frames elapses without detection of violations that satisfy the 13-bit criterion. Otherwise, 3 frames are required to indicate loss of synchronization. For both types of frames, the next 8 bits following the F/L pair constitute the first octet of data for the B1 channel. In the NT to TE direction, these bits are followed by an E bit and a D bit. The E bit is the echo channel for the D bits; upon receiving a D bit, the NT echoes it back to the TE(s) in the next E-bit position so the TEs may compare it to their own transmission for collision detection purposes. The first D bit is followed by the A bit, which is set when the interface is activated and synchronized. The A bit is followed by the auxiliary framing pair F_A and N, which are in turn followed by the first octet of data for the B2 channel. The second occurrence of an E and D bit is next, followed by the multiframing bit M. The remainder of the frame consists of the second octet of B1 data, the third E and D bit pair, the "S" bit (for further study), the second octet of B2 data, the fourth and final E and D bit pair, and the frame balance bit L. Note that the final frame balance bit L serves the dual purpose of DC balancing the entire frame as well as guaranteeing that the last MARK of the frame is a positive MARK.

The frame structure in the TE to NT direction is considerably different. The frame begins with an F/L pair as before, followed by the first octet of B1 data. However, the D bits are preceded by balance bits L so that the D bit may be restricted to either SPACE (no line signal) or negative MARK. This prevents the collision of negative MARKs with positive MARKs in the multipoint situation, which could result in a composite waveform resembling SPACE. Since the spacing condition is interpreted as line IDLE, the efficiency of the D-channel access procedures would be reduced. A key feature to note is that the L bits force the first MARK of each data octet to be negative MARK. This simplifies correct DC balancing during multipoint operation when the B1 and B2 data sources come from different TEs; if the TEs did not know which polarity of MARK to begin with, they could introduce erroneous code violations.

The first occurrence of a D bit is followed by a balance bit L, the F_A bit, and another L bit. The L bit preceding the F_A bit guarantees that the F_A bit can be a negative MARK, and the next L bit guarantees that the first MARK of the following B2 data octet can be a negative MARK. The rest of the frame follows a similar pattern for the remaining D and B bits. As before, the final L bit DC balances the frame and ensures that the F bit of the next frame will be a code violation.

D-CHANNEL PROCEDURES

The D-channel procedures allow multiple TEs to share the D channel in a multipoint configuration, or single TEs to operate in a point-to-point configuration.

When a TE has no Layer 2 frames to transmit, it sends binary ONEs on the D channel, which results in no line signal. When the NT has no Layer 2 frames to transmit, it may send binary ONEs or repeat HDLC flags. An LAPD flag is the octet "01111110," and defines the beginning or ending of an LAPD packet. A flag that closes a packet may also define the beginning of a new packet. To prevent the occurrence of the flag pattern in the actual data, the transmitter must include a "zero insertion" function that automatically inserts a ZERO after each sequence of five contiguous logical ONEs. Similarly, the receiver must include a "zero deletion" function that automatically deletes any ZEROs that follow five contiguous logical ONEs. Any occurrence of six logical ONEs in the received data will therefore indicate a flag. As discussed in the previous section, the NT will echo a received D bit in the next available E-bit position towards the TEs. The TEs will monitor the E-bit position, both to gain access to the D channel as well as to check for collision with other TEs. A TE that intends to transmit data must monitor the E bit, counting the number of consecutive binary ONEs. Once a count threshold corresponding to the priority of

the TE is reached, it may begin to transmit data. The priority level may be fixed for a particular TE, or it may be programmed after system powerup. The priority count is incremented following successful transmission of a packet to allow other TEs equal access to the channel. Typical priority counts range from eight and nine for signaling packets to ten and eleven for data packets. Once a TE begins D-channel transmission, it must monitor the E bit and compare it with its last transmitted D bit. If they match, transmission continues, otherwise a collision or line error has occurred and the TE must cease transmission and return to counting binary ONEs.

ACTIVATION/DEACTIVATION SEQUENCES

The I.430 specification defines a set of F states, numbered from F1 through F8, to indicate the state of the TE during activation and deactivation procedures. Similarly, a set of G states numbered from G1 through G4 are used to indicate the state of the NT. Section 6.2 of I.430 is included for reference at the end of this application note and defines the precise meaning of each F and G state. Also included is Table 2 of I.430, which describes the format of the "INFO" signals exchanged by TE and NT during the initialization sequence. Tables 3 and 4 of I.430 are appended to this note, and define state tables which indicate the state transitions to be made based upon events such as reception of particular INFO signals.

The meaning and sequence of states are clearly defined in the specification, but a few points require special note. Attention is drawn to the difference between the inactive and deactivated TE states. In the inactive state there is no power, and therefore nothing is happening in the TE. Consequently, the Am79C30A only provides indication of states F2 through F8. In the deactivated state, the TE has been placed in a low power state, but will monitor the line for an indication to activate or may request activation itself if requested to do so by higher TE software layers. Note also that a TE may request activation, but may not request deactivation. A TE distinguishes INFO2 from INFO4 by the state of the "A," or activation bit.

The "handshake" sequence of the F and G states is relatively forgiving, since the D-channel protocol must be satisfied before any actual data can be transmitted. For instance, in multipoint operation it is possible to have overlapping but unsynchronized INFO1 signals from TEs to NT. A single INFO1 signal consists of a continuous pattern of positive MARK, negative MARK, and six SPACEs. The composite signal may not resemble an individual INFO1, but the NT will respond with an INFO2 pattern and the individual TEs will then synchronize.

MULTIFRAMING

Multiframing is a mechanism that provides for the transmission of a Q bit in the TE to NT direction every fifth frame. The information is intended for the NT only; there is no requirement for the NT to transmit any information in the upstream direction to the exchange termination. It is intended to provide an additional low-speed channel from the TE to the NT. At the current time, the procedures and usage of the multiframe capabilities are not widely implemented. Section 7 of the ANSI document does, however, define some uses of the multiframing capability for maintenance functions.

If multiframing is supported, the Q-bit positions are identified by the setting of the F_A bit to a binary ONE in the NT to TE direction every fifth frame. This allows the TEs to synchronize their Q transmissions, preventing collision of F_A bits from one TE with the Q bits from another. However, there is no mechanism for Q-bit collision detection recovery between TEs. An additional feature is the setting of the M bit in the NT to TE direction every 20 frames, creating a multiframe structure that supports the transmission of 4-bit characters from TE to NT. A single S bit is transmitted each frame in the NT to TE direction.

The fact that systems have been designed while the standards were evolving can lead to situations where equipment may not respond exactly as expected. The case in point is when an NT transmits a logical "1" in the F_A position to an Am79C30A during the activation sequence. Although the NT should not consistently send "1" in this position, cases have been observed where this condition has indeed occurred. If multiframing is disabled in the Am79C30A, it will echo the received F_A bit back to the NT. If the B1 channel is disabled, or sends $FF, the TE and NT will fail to synchronize since the NT will not see a second code violation within the first 13 bits of the frame. A simple workaround for this situation is to enable multiframing (set Am79C30A MF register bit 0 to "1") and force the F_A response to be logical "0" (set Am79C30A MFQB register bit 4 to "0"). This guarantees that the F_A bit in the TE to NT direction will provide a code violation if the B1 channel data does not.

The Am79C30A provides full support for all multiframing functions. If multiframing is enabled, the DSC will monitor the received F_A and M bits to establish multiframe synchronization, buffer received S bits, and buffer Q bits for transmission synchronized to the received multiframe.

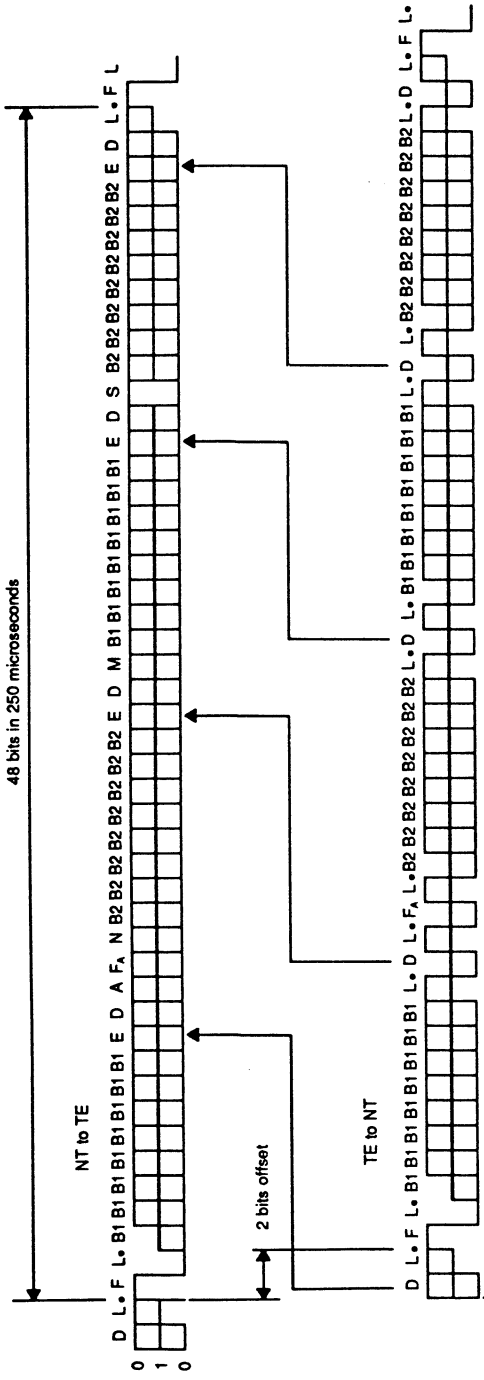
ELECTRICAL CHARACTERISTICS

Recommendation I.430 describes in detail the electrical testing requirements of the S and T interfaces. Areas covered include the allowable phase jitter and deviation allowed from TE input to output, the allowable jitter output of the NT, and the waveforms and test conditions under which these measurements are made. The NT and TE input and output impedance requirements are strictly specified, as is the shape of the output waveforms and performance objectives in the presence of noise. A

detailed treatment of electrical compliance is given in a companion application note on S and T Interface Circuitry.

POWER FEEDING ISSUES

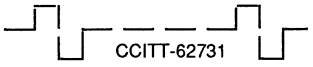
A key section of I.430 deals with the requirements for power feeding and consumption. Tight restrictions on power consumption are defined for telephones that are designated to operate in "restricted," or emergency power modes. For normal operation the power budget is more lenient, but a designer who wishes to add features to the basic telephone will need to plan power consumption carefully. These power targets create considerable challenges for IC and systems designers alike, and have a great impact on terminal design. Power issues are discussed in detail in companion notes on S and T Interface Power Issues.



Notes:
1. Dots demarcate those parts of the frame that are independently DC-balanced.
2. The F_A bit in the direction TE to NT is used as a Q-bit in every fifth frame if the Q-Channel capability is applied (see Section 6.3.3).
3. The nominal 2-bit offset is as seen from the TE (I_A in Figure 2/I.430). The corresponding offset at the NT may be greater due to delay in the interface cable and varies by configuration.

Figure 3/I.430. Frame Structure at Reference Points S and T

Table 2/I.430. Definition of INFO Signals (note 1)

Signals from NT to TE		Signals from TE to NT	
INFO 0	No signal	INFO 0	No signal
		INFO 1 (note 2)	A continuous signal with the following pattern: Positive ZERO, negative ZERO, six ONEs.  Nominal bit rate = 192 kbit/s
INFO 2 (note 3)	Frame with all bits of B, D, and D echo channels set to binary ZERO. Bit A set to binary ZERO. N and L bits set according to the normal coding rules.		
INFO 4 (note 3)	Frames with operational data on B, D, and D echo channels. Bit A set to binary ONE.	INFO 3	Synchronized frames with operational data on B and D channels.

Notes: 1. For configurations where the wiring polarity may be reversed (see Section 4.3), signals may be received with the polarity of the binary ZEROs inverted. All NT and TE receivers should be designed to tolerate wiring polarity reversals.

2. TEs that do not need the capability to initiate activation of a deactivated I.430 interface (that is, TEs required to handle only incoming calls) need not have the capability to send INFO 1. In all other respects, these TEs shall be in accordance with Section 6.2. It should be noted that in the point-to-multipoint configuration, more than one TE transmitting simultaneously will produce a bit pattern as received by the NT and different from that described above, that is, two or more overlapping (asynchronous) instances of INFO 1.

3. During the transmission of INFO 2 or INFO 4, the F_A bits and the M bits from the NT may provide the Q-bit pattern designation as described in Section 6.3.3.

Table 3/I.430. Activation/deactivation Layer 1 Finite State Matrix for TEs Powered from Power Source 1 or 2

State Name / Number / Event / INFO	Inactive F1 INFO 0	Sensing F2 INFO 0	Deacti-vated F3 INFO 0	Awaiting signal F4 INFO 1	Identi-fying input F5 INFO 0	Synchro-nized F6 INFO 3	Activated F7 INFO 3	Lost framing F8 INFO 0
Power on and detection of Power 2 (notes 2 and 3)	F1	—	—	—	—	—	—	—
Loss of power (note 2)	—	F1	MPH-II(d) F1	MPH-II(d) MPH-DI PH-DI F1	MPH-II(d) MPH-DI PH-DI F1	MPH-II(d) MPH-DI PH-DI F1	MPH-II(d) MPH-DI PH-DI F1	MPH-II(c) MPH-DI PH-DI F1
Disappearance of Power S (note 3)	—	F1	MPH-II(d) F1	MPH-II(d) MPH-DI PH-DI F1	MPH-II(d) MPH-DI PH-DI F1	MPH-II(d) MPH-DI PH-DI F1	MPH-II(d) MPH-DI PH-DI F1	MPH-II(c) MPH-DI PH-DI F1
PH Act Req	/	|	ST.T3 F4	|	|	—	|	—
Expiry T3	/	/	—	MPH-DI PH-DI F3	MPH-DI PH-DI F3	MPH-DI PH-DI F3	—	—
Rec. INFO 0	/	MPH-II(c) F3	—	—	—	MPH-DI PH-DI F3	MPH-DI PH-DI F3	MPH-DI PH-DI MPH-EI1 F3
Rec. any signal (note 1)	/	—	—	F5	—	/	/	—
Rec. INFO 2	/	MPH-II(c) F6	F6	/	F6	—	MPH-EI1 F6	MPH-EI1 F6
Rec. INFO 4	/	MPH-II(c) PH-AI MPH-AI F7	PH-AI MPH-AI F7	/	PH-AI MPH-AI F7	PH-AI MPH-AI MPH-EI2 F7	—	PH-AI MPH-AI MPH-EI1 F7
Lost framing	/	/	/	/	/	MPH-EI1 F8	MPH-EI1 F8	—

Notations

—	No change, no action
/	Impossible situation
|	Impossible by the definition of the Layer 1 service
a, b; F*n*	Issue primitives "a" and "b" and then go to state "F*n*"
PH-AI	Primitive PH-Activate Indication
PH-DI	Primitive PH-Deactivate Indication
MPH-AI	Primitive MPH-Activate Indication
MPH-DI	Primitive MPH-Deactivate Indication
MPH-EI1	Primitive MPH-Error Indication reporting error
MPH-EI2	Primitive MPF-Error Indication reporting recovery from error
MPH-II(c)	Primitive MPH-Information Indication (connected)
MPH-II(d)	Primitive MPH-Information Indication (disconnected)
ST.T3	Start timer T3
Power S	Power Source 1 or Power Source 2

Table 4/I.430. Activation/deactivation Layer 1 Finite State Matrix for NTs

Event \ State Name / Number / INFO	Inactive G1 INFO 0	Pending activation G2 INFO 2	Active G3 INFO 4	Pending deactivation G4 INFO 0
Power on and detection of power S	F2			
PH-Act Req	Start timer T1 G2	—	|	Start timer T1 G2
MPH-Deact Req	|	Start timer T2 PH-DI; G4	Start timer T2 PH-DI; G4	|
Expiry T1 (note 1)	—	Start timer T2 PH-DI; G4	/	—
Expiry T2 (note 2)	—	—	—	G1
Receiving INFO 0	—	—	MPH-DI; MPH-EI G2 (note 3)	G1
Receiving INFO 1	Start timer T1 G2	—	/	—
Receiving INFO 3	/	Stop timer T1 PH-AI; MPH-AI G3 (note 4)	—	—
Lost framing	/	/	MPH-DI; MPH-EI G2 (note 3)	—

Notations

—	No state change
/	Impossible by the definition of peer-to-peer physical layer procedures or system internal reasons
|	Impossible by the definition of the physical layer service
a, b; G*n*	Issue primitives "a" and "b" and then go to state "G*n*"
PH-AI	Primitive PH-Activate Indication
PH-DI	Primitive PH-Deactivate Indication
MPH-AI	Primitive MPH-Activate Indication
MPH-DI	Primitive MPH-Deactivate Indication
MPH-EI	Primitive MPH-Error Indication

Primitives are signals in a conceptual queue and will be cleared on recognition, while the INFO signals are continuous signals that are available all the time.

Notes: 1. Timer 1 (T1) is a supervisory timer that has to take into account the overall time to activate. This time includes the time it takes to activate both the ET-NT and the NT-ET portion of the customer access. ET is the exchange termination.

2. Timer 2 (T2) prevents unintentional reactivation. Its value is 25 ms ≤ value ≤ 100 ms. This implies that a TE has to recognize INFO 0 and to react on it within 25 ms. If the NT is able to unambiguously recognize INFO 1, then the value of timer 2 may be 0.

6.2 Activation/deactivation

6.2.1 Definitions

6.2.1.1 TE states

6.2.1.1.1 STATE F1 (inactive): In this inactive state the TE is not transmitting. In the case of locally powered TEs that cannot detect the appearance/disappearance of Power Source 1 or 2, this state is entered when local power is not present. For TEs that can detect Power Source 1 or Power Source 2, this state is entered whenever loss of power (required to support all TEI functions) is detected, or when the absence of power from Source 1 or 2, whichever power source is used for determining the connection status, is detected.

6.2.1.1.2 STATE F2 (sensing): This state is entered after the TE has been powered on but has not determined the type of signal (if any) that the TE is receiving.

6.2.1.1.3 STATE F3 (deactivated): This is the deactivated state of the physical protocol. Neither the NT nor the TE is transmitting.

6.2.1.1.4 STATE F4 (awaiting signal): When the TE is requested to initiate activation by means of a PH-Activate Request primitive, it transmits a signal (INFO 1) and waits for a response from the NT.

6.2.1.1.5 STATE F5 (identifying input): At the first receipt of any signal from the NT, the TE ceases to

transmit INFO 1 and awaits identification of signal INFO 2 or INFO 4.

6.2.1.1.6 STATE F6 (synchronized): When the TE receives an activation signal (INFO 2) from the NT, it responds with a signal (INFO 3) and waits for normal frames (INFO 4) from the NT.

6.2.1.1.7 STATE F7 (activated): This is the normal active state with the protocol activated in both directions. Both the NT and the TE are transmitting normal frames.

6.2.1.1.8 STATE F8 (lost framing): This is the condition when the TE has lost frame synchronization and is awaiting re-synchronization by receipt of INFO 2 or INFO 4, or deactivation by receipt of INFO 0.

6.2.1.2 NT states

6.2.1.2.1 STATE G1 (inactive): In this deactivated state, the NT is not transmitting.

6.2.1.2.2 STATE G2 (pending activation): In this partially active state, the NT sends INFO 2 while waiting for INFO 3. This state will be entered on request by higher layers by means of a PH-Activate Request primitive, or on the receipt of INFO 0 or lost framing while in the active state (G3). Then the choice to eventually deactivate is up to higher layers within the NT.

6.2.1.2.3 STATE G3 (active): This is the normal active state where the NT and TE are active with INFO 4 and INFO 3, respectively. A deactivation may be initiated by the NT system management by means of an MPH-Deactivate Request primitive, or the NT may be in the active state all the time, under non-fault conditions.

6.2.1.2.4 STATE G4 (pending deactivation): When the NT wishes to deactivate, it may wait for a timer to expire before returning to the deactivated state.

CCITT G.714 CODEC Testing Tutorial

The incorporation of ISDN voice capabilities into terminal and computer equipment presents many engineers with new terminology and testing ideas. A brief overview of CCITT Recommendation G.714 is helpful in gaining familiarity with the concepts of codec performance testing.

INTRODUCTION TO G.714

There does not yet exist a single comprehensive CCITT recommendation for testing codec and audio performance in the ISDN environment, and many systems vendors are using selected portions of CCITT G.714 as a basis for evaluating components. In fact, the transmission characteristics of the Am79C30A datasheet are based upon G.714. As will be seen in the following sections, only portions of G.714 are applicable to ISDN ICs, since G.714 was defined to specify performance of A/D and D/A conversions in a four-wire central office trunk environment. In such mixed analog and digital systems, a voice signal may pass through multiple A/D and D/A conversions; for instance, a signal may spend part of its time on analog frequency division multiplexed microwave channels and part of its time on digital T1 channels. Because of the wide variation in analog phone line characteristics and the cumulative effects of multiple A/D and D/A conversions, G.714 is a fairly stringent specification. Introduced in 1984 as an extension to the 1972 CCITT G.712 recommendation, G.714 specifies performance for send and receive sides (half channels) separately whereas G.712 specifies the performance of PCM connections from analog port to analog port (full channel). The intention is that any combination of transmitter and receiver that meet G.714 will be guaranteed to meet G.712 when cascaded, avoiding the possibility of offsetting errors in sender and receiver. At the current time, G.714 is applied to the ISDN environment due to the lack of a more relevant specification; it is expected that evolving CCITT recommendations will specify the requirements of the ISDN environment as a combination of codec performance and handset acoustics.

The introductory section of G.714 defines two terms that are used in the recommendation. A "standard send side" is a hypothetical ideal A/D converter preceded by an ideal low-pass filter. Similarly, a "standard receive side" is a hypothetical ideal D/A converter followed by an ideal low-pass filter. Typically, these devices are simulated by digital transmission test sets. Furthermore, where a nominal reference frequency of 1000 Hz is mentioned, the actual frequency chosen should be in the range of 1004 to 1020 Hz.

SECTION 2: ADJUSTMENT OF RELATIVE LEVELS

Section 2 of G.714 specifies the adjustment of absolute gain and load capacity. To measure the absolute gain of the transmitter, a 0-dBm0 analog signal at a nominal frequency of 1000 Hz is applied to the input, and the PCM output level must be 0 ± 0.3 dBm0. The 0-dBm0 level is approximately 3 dB below the peak PCM code and is intended to represent the normal peak signal level. The extra 3 dB is to allow some headroom to prevent clipping under normal operating conditions. It is important to note that "dBm0" is a relative measure; the exact rms voltage corresponding to the 0-dBm0 level varies from one system to another. In an analog transmission system environment, the 0-dBm0 point is chosen to represent a desired relation between the PCM codes on the codec digital interface and the corresponding analog levels on the system trunk interface. In an ISDN environment, the digital and analog conversions take place in a telephone environment and not a trunk environment. The absolute gain measurement is often applied as a component specification of part-to-part variation, but a true system specification for the ISDN environment would provide a specific relation between PCM codes on the codec digital interface and the corresponding acoustic levels on the telephone handset. It is crucial to carefully consider the scope and applicability of system specifications when applying them as component specifications.

The load capacity for the transmitter is checked by applying a sine wave of nominal frequency, 1000 Hz, to the input, and increasing the input level until the first occurrence of both the positive and negative full-scale PCM values. A value of 0.3 dB is added to this input level to compensate for the last PCM step, and the resultant value should be within ±0.3 dB of the theoretical full scale.

The receive side absolute gain is checked by applying a sequence of PCM codes corresponding to a 0-dBm0 sine wave, and verifying that the resultant analog output level is 0 ±0.3 dBm0.

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SECTIONS 3, 4, 5, AND 6

Section 3 of G.714 describes level measurement stability requirements with respect to power supply and temperature variations, but does not specify the actual permitted variations. Careful selection of both active and discrete components should guarantee compliance with this system specification.

Sections 4 and 5 of G.714 specify the nominal four-wire input and output impedance, return loss, and longitudinal balance requirements of analog lines—parameters that are not directly relevant to the ISDN environment. Similarly, Section 6 deals with the signal levels that should be present at the interface between a four-wire trunk and frequency division multiplexed equipment, which is obviously not directly relevant to the ISDN application.

SECTIONS 7 AND 8: ATTENUATION AND GROUP DELAY

Section 7 of G.714 specifies a template for gain versus frequency performance, which is illustrated in Figure 2/G.714 at the end of this application note. It may be seen that this template is relatively flat between 300 and 2400 Hz, the usable audio range. Increased attenuation is allowed below 200 Hz to help filter 50- and 60-Hz power-supply harmonics, and the requirements are relaxed above 2400 Hz to allow a low-pass filter roll-off to be implemented in a practical fashion. The test is performed at a preferred power level of –10 dBm0, although 0 dBm0 is considered acceptable. The nominal 0-dB reference point is at 1000 Hz.

Section 8 of G.714 specifies a template for group delay distortion, and also specifies that the absolute group delay for transmitter and receiver should not exceed 360 and 240 microseconds, respectively, when measured at the frequency that has minimum group delay. The template allows for increased group delay at the upper and lower limits of the voiceband to allow out-of-band attenuation requirements to be met with simpler filters. As in the previous test, the preferred input power level is –10 dBm0, but 0 dBm0 is an acceptable alternative. The group delay distortion template is illustrated in Figure 3/G.714 on page 16.

SECTIONS 9–13: NOISE MEASUREMENT

Section 9 of G.714 specifies that with the input of the send side terminated with a nominal 600-ohm impedance, the measured idle channel noise should not exceed –66 dBm0p. Similarly, Section 10 states that the noise contributed by the receiver should not exceed –75 dBm0p when its input is driven by either PCM 0 (μ-law) or PCM 1 (A-law). A value of –75 dBm0p means that the noise should be attenuated 75 dB relative to the 0-dBm0 point, and adjusted by a psophometric noise weighting curve. The psophometric curve is widely used in Europe to combine the filtering effects of telephone handsets and subjective human hearing response. In North America, a different curve called "C-message weighting" is used for the same purpose.

Sections 11 and 12 of G.714 define limits for the rejection and prevention of out-of-band noise. Section 11 requires that any sine wave of frequency greater than 4.6 kHz at the input of the send side should not result in any in-band signal greater than 25 dB below the level of the test signal. Furthermore, "under the most adverse practical network conditions" of out-of-band noise, the PCM channel should not contribute more than 100 pWOp of additional noise in the band 0–4 kHz at the channel output. This requirement is intended as a guideline and is not applicable as a component specification since the test conditions are not explicit. The unit pWOp refers to picoWatts of power, referenced to the 0-dBm point and adjusted by a psophometric noise filter. For the receive side, Section 12 indicates that a 0-dBm0 digitally simulated sine wave in the range of 300 to 3400 Hz should not result in any spurious out-of-band image signals greater than –25 dBm0.

In addition to the total noise power specifications, Section 13 requires that no single frequency from the send or receive side should exceed –50 dBm0.

SECTIONS 14 AND 15: STD AND GAIN TRACKING

For signal-to-distortion testing, Section 14 of G.714 recommends two alternative methods that are not exactly equivalent: sine wave testing (Method 2) and noise-based testing (Method 1). It is stated that Method 1 "gives fairly smooth curves, not very dependent upon input signal level. The sine wave method can be more sensitive in identifying possible localized codec imperfections. Thus the two methods respond to practical codec impairments in slightly different ways." The G.714 specification allows regulatory administrations to choose between either or both of these methods. For sine wave testing, the test signal used is a nominal 420-, 820-, or 1020-Hz waveform. For noise-based testing, a particular pseudorandom sequence of tones is used. There are two different templates for send and receive in noise-based testing, whereas a single template applies for sine wave testing.

A similar situation exists for the measurement of gain variation with respect to input level, commonly referred to as gain tracking. A choice is given between noise-based testing or sine wave testing, with different templates for each method.

The various templates for STD and gain tracking are attached in G714 Figures 4a, 4b, 5, 6, and 7.

SECTIONS 16–18: CROSSTALK AND SIGNALING

Since G.714 was written to specify four-wire analog trunks, a variety of crosstalk tests are defined in Sections 16 and 17 to limit the crosstalk between send and receive channels, and between individual channels of a multiplex group. These measurements do not directly apply to the ISDN environment. Moreover, in a telephone application, the designer will deliberately mix a large sidetone signal into the receive path from the transmit path.

Section 18 of G.714 deals with interference from signaling, which is not directly relevant to the ISDN environment.

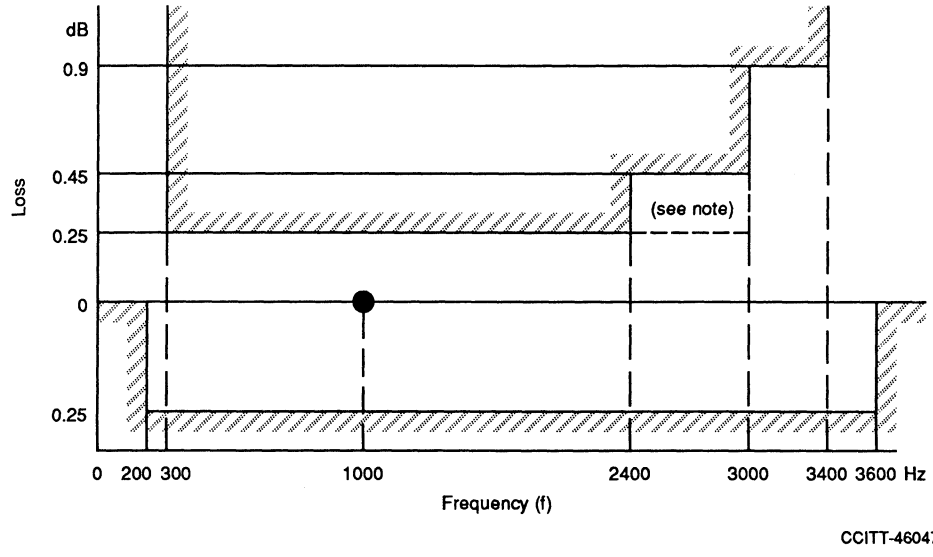


Figure 2/G.714. Attenuation/Frequency Distortion

Note: In some applications in which several PCM channels may be connected in tandem, it may be necessary to extend the +0.25-dB limit from 2400 Hz to 3000 Hz.

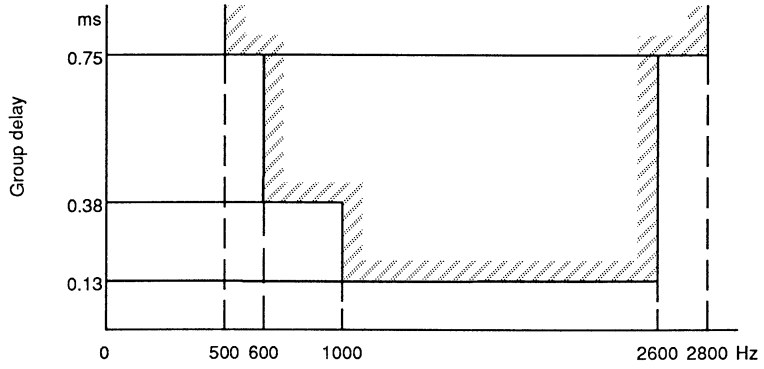


Figure 3/G.714. Group Delay Distortion with Frequency

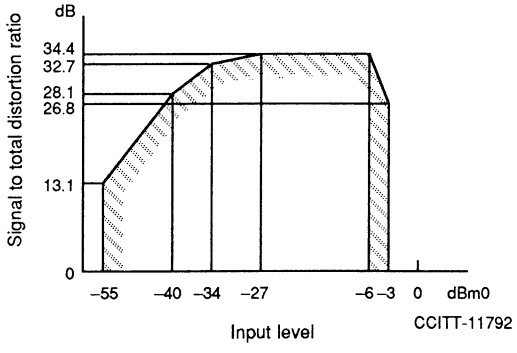


Figure 4a/G.714. Signal-to-Total Distortion Ratio as a function of Input Level (Method 1), Send Side

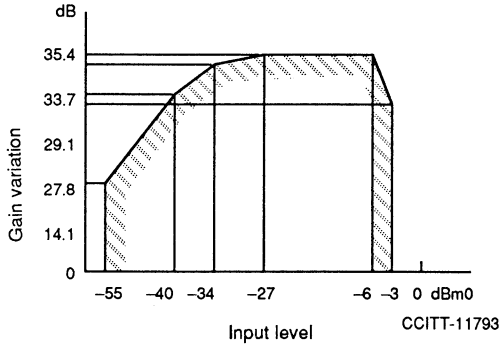


Figure 4b/G.714. Signal-to-Noise Distortion as a function of Input Level (Method 1), Receive Side

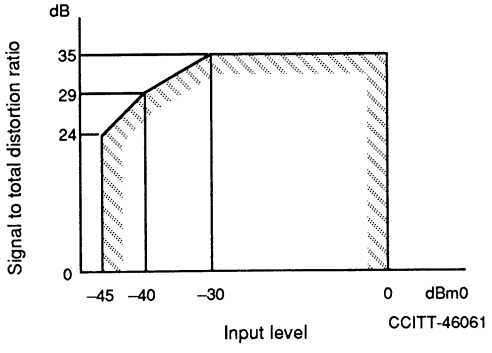


Figure 5/G.714. Signal-to-Total Distortion as a Function of the Input Level (Method 2), Send and Receive Side

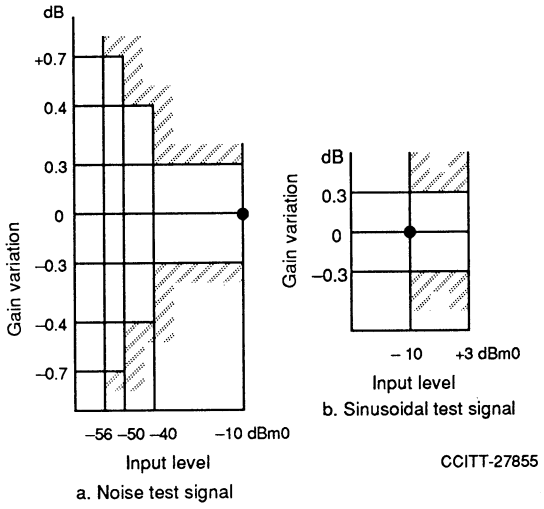


Figure 6/G.714. Variation of Gain with Input Level (Method 1)

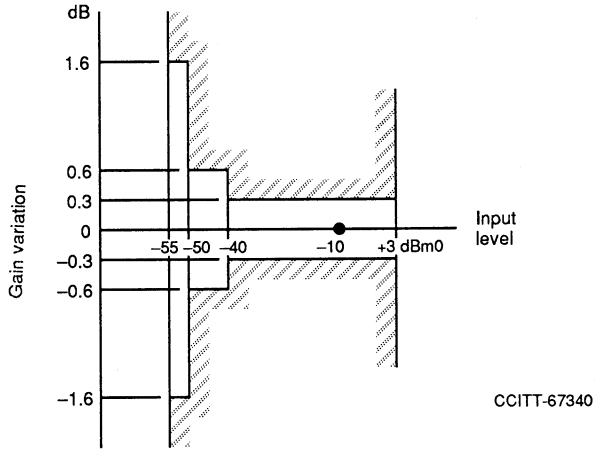


Figure 7/G.714. Variation of Gain with Input Level (Method 2)

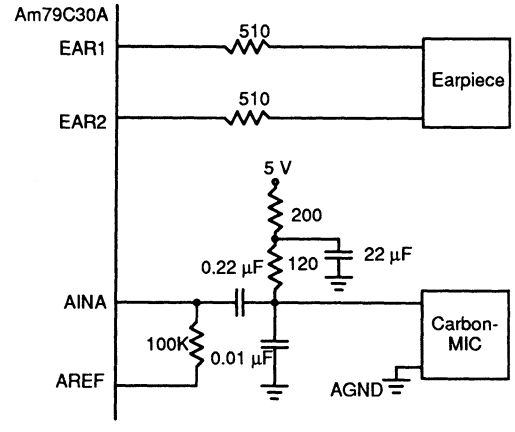
Am79C30A Carbon Handset Interface

The carbon-type microphone was for many years the standard choice for telephone design. Although it is being supplanted by electret and dynamic microphones, the carbon microphone still offers advantages of user acceptance, mechanical reliability, and ease of interface.

The accompanying schematic illustrates that a carbon handset may be interfaced to the Am79C30A DSC using only a few discrete components. The receive path from the DSC EAR1 and EAR2 outputs to the handset speaker is particularly simple, consisting of a pair of 510-ohm resistors. A pair of resistors was chosen instead of a single 1.1-kohm resistor to provide current limiting protection on both EAR outputs in case the user connects something other than a handset to the connector. The 510-ohm series resistors were selected to provide a subjective comfortable listening level with the DSC gains set at 0 dB. This design was implemented using an ITT 6544-0M2 handset, and it is important to note that the series resistor values may vary depending upon the handset manufacturer. Some further adjustment of the series resistance may be needed for compliance with applicable sound pressure level tests, depending upon the application. Note that the total resistance seen between the EAR1 and EAR2 outputs must be greater than 540 ohms, which is the maximum drive capability of the EAR outputs. The LS outputs are provided for lower impedance loads, such as loudspeakers, and are capable of driving a 40-ohm load. The GER filter of the DSC may be used for volume control, but it is desirable to center the desired volume level using the external resistance to make optimum use of the dynamic range of the digital signal processing.

In the transmit path, the gain of the carbon microphone is determined by the series combination of the 120-ohm and 200-ohm resistors, which set the bias current provided to the microphone. As was the case for the earpiece, the gain was set to provide a subjective comfortable volume level, and may require adjustment for a different manufacturer or if the application requires specific acoustic testing.

In all microphone circuits for the Am79C30A DSC, it is critical to ensure that the external circuitry does not contribute noise in the audio band. This is particularly true in personal computer applications, since the power supplies tend to be very noisy. The 200-ohm resistor and the 22-microfarad capacitor form a low-pass filter for the +5-V power supply, which reduces supply noise that would otherwise appear at the AINA input. If the power supply was quiet, the RC network would not be required and the 120-ohm and 200-ohm resistors could be replaced by a single 320-ohm resistor. The .01-microfarad capacitor is intended to filter out high-frequency noise from the microphone and is optional. The 0.22-microfarad capacitor provides DC blocking so that the 100-kohm resistor may bias the AINA input from the analog reference AREF.



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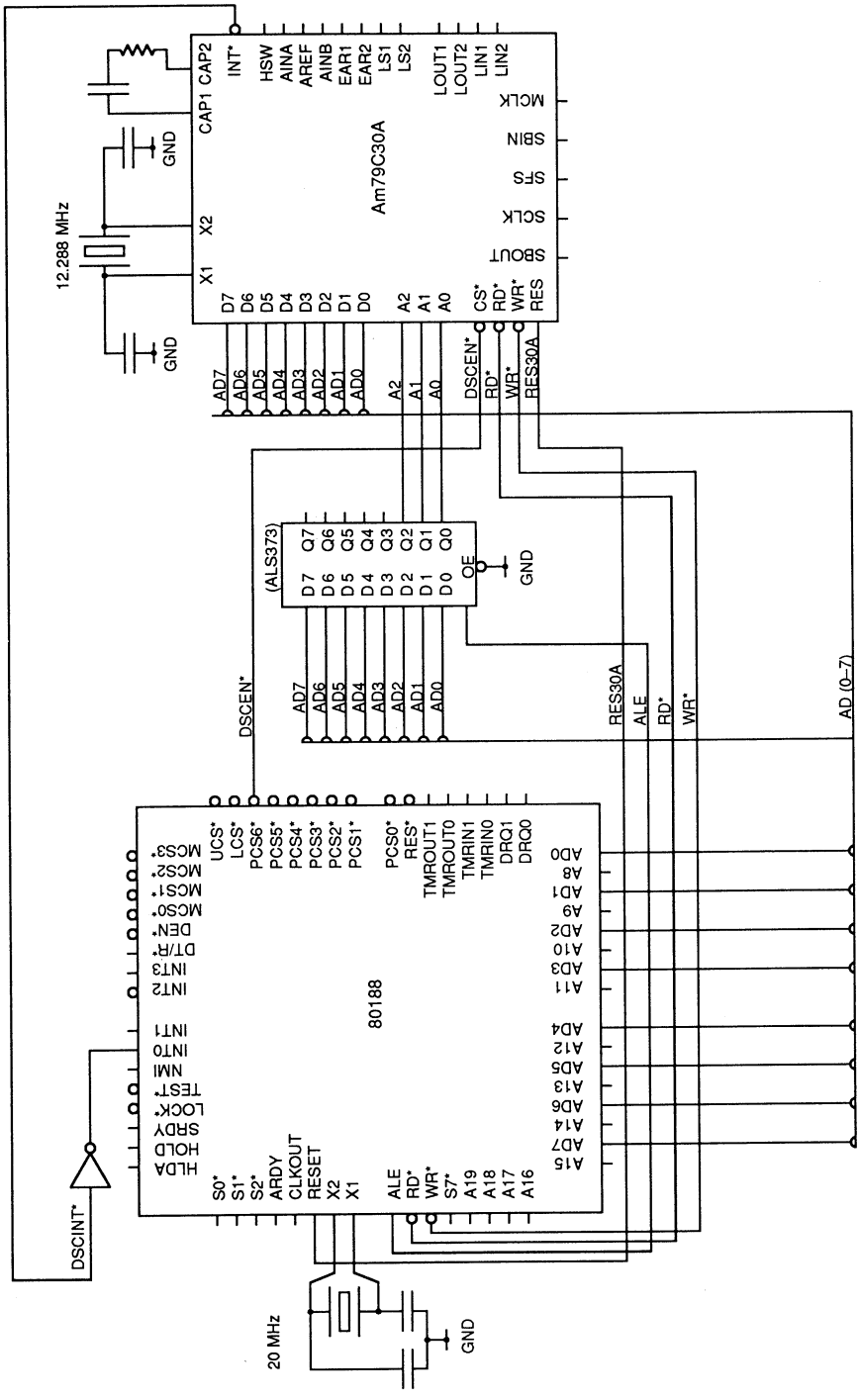
Am79C30A 80188 Microprocessor Interface

The 80188 is an excellent choice of microprocessor to use in conjunction with the Am79C30A DSC, since it integrates several useful peripherals and provides sufficient processing power to easily handle D-channel signaling and data processing. Spare processor bandwidth may be used to implement data processing capability for a B channel or to add other system features.

The accompanying schematic illustrates the key components that are required to interface the 80188 microprocessor to the Am79C30A DSC. The Am79C30A presents an iAPX-type interface, thus the DSC connects virtually directly to the microprocessor system. The 8-bit data bus is directly connected between the DSC and the microprocessor; the CMOS design of the DSC and the high drive capability of the 80188 microprocessor make extra bus buffering unnecessary for most systems. The RD* and WR* control signals are also directly connected between the microprocessor and the DSC. A '373-type transparent latch strobed by the processor's ALE signal is used to demultiplex the low-order address bits, and the 3 least significant output bits of this latch are connected to the DSC. Generally, 80188-based systems require this demultiplexing latch to interface to other peripherals and memory. The interrupt output of the DSC is active LOW, which necessitates an inverter before connection to an 80188 interrupt input. The DSC reset is provided by the reset output of the processor. The DSC chip select is provided by a peripheral chip select line from the 80188 microprocessor. The RD* and WR* minimum LOW time for the DSC is 200 ns, which requires the peripheral chip select line to be programmed for insertion of one processor wait state for 10-MHz operation. The DSC crystal in this application diagram is Saronix part number NYP-122-20, used in conjunction with two 30-pF load capacitors. If 10-MHz processor operation is not required, the DSC MCLK output may be used as the clock source for the processor to provide a wide range of frequencies under software control.


Am79C30A
CAP2
CAP1
X2
X1
INT*
HSW
AINA
AREF
AINB
EAR1
EAR2
LS1
LS2
LOUT1
LOUT2
LIN1
LIN2
MCLK
SBIN
SFS
SCLK
SBOUT
D7
D6
D5
D4
D3
D2
D1
D0
A2
A1
A0
CS*
RD*
WR*
RES
GND
12.288 MHz
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
DSCEN*
RES30A
(ALS373)
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
OE
ALE
AD (0–7)
80188
UCS*
LCS*
PCS6*
PCS5*
PCS4*
PCS3*
PCS2*
PCS1*
PCS0*
RES*
TMROUT1
TMROUT0
TMRIN1
TMRIN0
DRQ1
DRQ0
MCS3*
MCS2*
MCS1*
MCS0*
DEN*
DT/R*
INT3
INT2
INT1
INT0
NMI
TEST*
LOCK*
SRDY
HOLD
HLDA
S0*
S1*
S2*
ARDY
CLKOUT
RESET
S7*
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
DSCINT*
20 MHz

ISDN Reference Model Tutorial

The ISDN reference model provides a topographical map of the network from the user to the telephone company's switch. This map identifies equipment types and "reference points" throughout the network.

BACKGROUND

The basic structure of the Integrated Services Digital Network (ISDN) is specified in the CCITT I.411 recommendation. The network architecture is rooted in the existing analog telephone network, in that the digital portions of the present telephone network are based on a 64-kb/s channel, where voice is digitized as 8000 8-bit words per second. In general ISDN retains this basic 64K rate, but allows it to be used for either voice or data.

ISDN service is divided into two classes, basic rate and primary rate. The basic rate service provides two 64-kb/s channels for either voice or data—referred to as bearer, or B, channels, and a 16-kb/s signaling/data channel, labeled the D channel, for call control and low speed, up to 9600-b/s packet data. This "2B plus D" capability is the standard service provided to the user, that is, a telephone jack on the office wall provides the basic rate interface. Primary rate service provides a combination of 23 B channels and one 64-kb/s D channel (in Europe, primary rate service is 30 B channels plus one D channel because the European inter-office trunk network is based on a 2.048-megabit-per-second data rate instead of the 1.544-megabit-per-second rate used in North America). This "23B plus D" service is used primarily to connect PABXs to central offices and mainframe (or mini) computers. The general idea is that the B channels from all of the basic rate interfaces are gathered by the switch, PABX, or central office (Centrex service) and (1) routed within the switch to other local basic rate interfaces, (2) routed to distant basic rate interfaces via other switches and primary rate inter-switch trunk lines, or (3) concentrated and routed to a local or remote computing facility via primary rate lines. There are other options, such as providing primary rate service to the user's desk, but the options listed above are the predominant configurations.

The bandwidth of the primary rate interface can be partitioned in ways other than 23B plus D. For instance, one D channel can support its associated 23 B channels plus 24 B channels from each of an additional three primary rate interfaces. Alternately, the bandwidth of the primary rate channel can be partitioned into four 384-kb/s "H0" channels, or one 1.536-megabit-per-second "H11" channel (1.92-megabit-per-second "H12" in Europe). H0 channels can be used in combination with 64-kb/s B channels on the same primary rate line.

ISDN LANDSCAPE

Independent of whether basic or primary rate service is provided, the network topography from the desk top to the switch is the same. Figure 1 shows this topography, identifying specific classes of equipment that make up the network. In addition, certain "reference points" are defined that represent various interfaces. At each of these reference points the CCITT has established, or is in the process of establishing, standards for both hardware and software.

EQUIPMENT CLASSIFICATION

The equipment that makes up the network is classified based on function and location within the network. Starting from the network and moving toward the user we have the Line Termination (LT), which is located in the telephone company's switch, often at the central office. The LT performs Layer 1 functions for B and D channels, plus D-channel Layer 2 and 3 functions. Directly downstream of the LT is the Network Termination (NT). There are two types of NTs: NT1 and NT2. The NT1 performs such functions as line-length extension (repeaters) and two- to four-wire conversion (U to S interface). A key characteristic of NT1 devices is that they only deal with Layer 1 of the OSI seven-layer model. NT2s are intelligent, and actively participate in the call routing/control process. PABXs and line concentrators are examples of NT2 devices (a PABX actually contains both an NT1 and an NT2, with the T reference point being contained internal to the switch). Additionally, NT2 devices can be connected to multiple types of ISDN lines simultaneously. One important aspect of NT devices is that they often form the boundary between equipment owned by the customer and equipment owned by the telephone company. Farther downstream is the Terminal Equipment (TE). TEs represent computers, telephones, data terminals, and so on that are directly compatible with the ISDN. The last class of equipment is the Terminal Adapter (TA). TAs are the "box modems" of the ISDN

world. They provide for the connection of non-ISDN-compatible equipment to the network, that is, existing equipment.

REFERENCE POINTS

R Reference Point—The R reference point establishes the boundary between non-ISDN-compatible equipment and the network. Terminal Adapters (TA) are used to convert the communication protocol used by the non-ISDN-compatible terminal to the desired basic rate or primary rate protocol. It should be mentioned at this point that the network does not specify the data protocol used on either the B or H channels; all the network sees is a stream of bits. As a practical matter, however, standard protocols such as V.110, V.120, and X.25 will be used.

S Reference Point—The S reference point provides the connection between the NT2 equipment and the terminal (TE) or terminal adapter (TA). If no NT2 is present, there is no S reference point. In this case the TE or TA is connected directly to an NT1 device, and the interface is designated as a T reference point. Both primary rate and basic rate services can be provided at the S reference point.

It should be noted that it is common to refer to the four-wire basic rate service specified by CCITT recommendation I.430 as S interface service. While it is true that the S reference point is most often implemented in this way, a two-wire basic rate interface or primary rate interface can also be used at the S reference point. Additionally, the four-wire interface can be used to provide the U reference point. To keep the ISDN "alphabet soup" straight, it is important to remember that the various reference points identify the connection points between equipment classes and not the specific implementation or protocol of the interconnection.

T Reference Point—In addition to the connection of TAs and TEs to NT1 equipment, the T reference point provides the connection between an NT1 and an NT2. In a PABX, for example, the line circuit that connects to the network in the upstream direction (U reference point) provides the NT1 function, and the line circuit that connects to the TE or TA equipment (S reference point) provides the NT2 function. The T reference point in this case is internal to the PABX.

U Reference Point—The U reference point connects the LT to the NT1. Normally, a two-wire basic rate interface or a primary rate line is used, but the four-wire basic rate interface can also be used.

NETWORK TIMING

System Clock—The entire digital portion of the telephone network is synchronized to a master clock. This clock is passed from toll offices to central offices to PABXs down to the terminal equipment. This upstream to downstream flow of clocking information is required to maintain constant data rates throughout the network. It is the responsibility of any downstream device to recover the network clock from the data coming from the upstream switch. Data that is transmitted farther downstream is transmitted synchronously with respect to this recovered clock.

Slave/Slave Applications—A clock synchronization problem can arise on the trunk side of NT2 devices (side connected to the upstream device). The Layer 1 transceiver on the trunk-side line card recovers the network clock from the data on the line from the central office (this is how the PABX synchronizes to the network clock). The line card is said to be a "slave" to the network. The line card is also connected to the PABX's internal data highway (PCM Highway), which provides its own clock. Thus, the line card is also a "slave" to the PCM Highway. A synchronization problem exists since these two clocks are not necessarily locked in phase and frequency. To resolve this conflict, data buffering must be provided on the line card to absorb the mismatch.

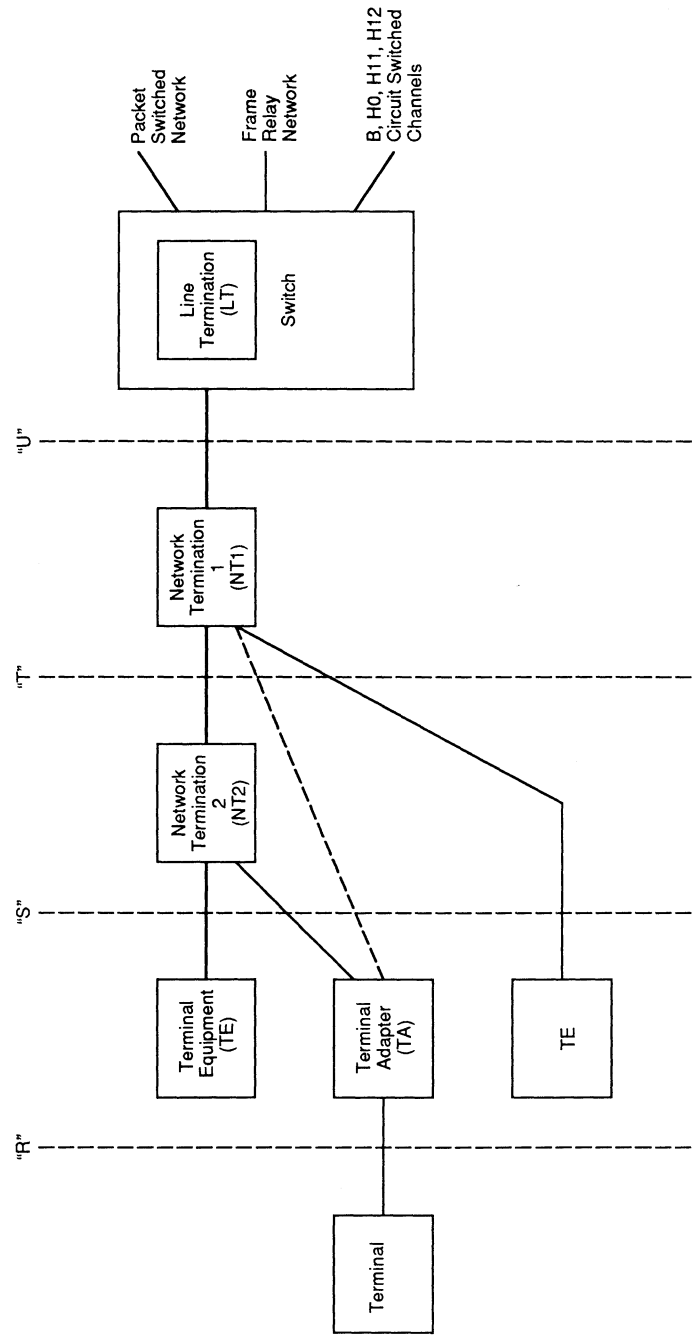


Figure 1. ISDN Network Topography

Am79C30A/32A DSC FIFO Handling

The Am79C30A Digital Subscriber Controller contains 2 data FIFOs and 3 status FIFOs to improve the throughput of packet transmission and reception. While the basic operation of the FIFOs is straightforward, there are some "tunable" parameters that can be programmed to increase performance.

GENERAL FIFO OPERATION

The Am79C30A Digital Subscriber Controller (DSC) has two 8-byte data FIFOs: one for the transmission of data and one for the reception of data. In addition to the data FIFOs there are three 2-byte-deep status FIFOs; the D-Channel Receive Byte Count Register (DRCR), the Address Status Register (ASR), and the D-Channel Error Register (DER). These 2-byte status FIFOs make it possible to receive two back-to-back data packets. The data FIFOs are very useful in the transmission and reception of LAPD packet data via the ISDN S interface. In this scenario the minimum and maximum packet sizes are defined, but the actual length of the packets may vary between these two extremes. During data transmission, the packet data is initially stored in local RAM and the processor is used to move the data from memory into the DSC transmit FIFO. When packet reception is in progress, the processor is used to move data from the DSC receive FIFO into local memory. Except for the initial 8 bytes loaded into the transmit FIFO, all FIFO servicing is handled from an interrupt service routine. Due to the importance of receiving and transmitting data, FIFO handling is given top priority in the interrupt service routine.

To be able to transmit and receive data packets longer than 8 bytes, some mechanism must be available to efficiently fill and empty the FIFOs. The solution provided by the Am79C30A DSC is programmable thresholds. When the number of bytes in the transmit FIFO is reduced to a preprogrammed level as a result of data transmission, an interrupt is generated to alert the processor to the fact that the FIFO needs to be filled. Similarly, when the number of bytes in the receive FIFO grows to a preprogrammed level as a result of data reception, the processor is alerted to the fact that the FIFO needs to be emptied.

The values that may be programmed into the transmit FIFO threshold are 1, 2, 4, or 8 empty bytes. The values that may be used for the receive FIFO threshold are 1, 2, 4, or 8 bytes. A good way to handle data transmission through the FIFO is as follows. At the start of a packet transmission, the transmit FIFO is initially filled with 8 bytes of data, and transmission is started by writing the Transmit Byte Count Register. One point to be emphasized here is that if the Transmit FIFO is initially loaded with a number of bytes less than or equal to the Transmit Threshold, a Transmit Threshold interrupt will be generated when the Transmit Byte Count is written. In all other cases, the threshold interrupts occur only when the number of bytes contained in the FIFO changes to the level programmed in the threshold register. In the case where the transmit FIFO threshold is programmed to 4 empty bytes, a Transmit Threshold interrupt is generated after 4 bytes have been transmitted, indicating that there are now 4 empty bytes in the transmit FIFO. The DSC transmitter does not stop transmission, so the processor must begin filling the FIFO within four byte-transmission times (approximately 2 milliseconds) or underrun will occur. When the processor is refilling the FIFO, it performs write operations until bit 4 of the D-Channel Status Register 2 (Transmit Buffer Available) indicates that the FIFO is completely full. At this point, the interrupt service routine is exited, and the processor is free to perform other functions. See the sample source code for the Transmit FIFO Handler later in this technical note.

In the situation where the receive FIFO threshold is 4 bytes, an interrupt will be generated to the processor after 4 bytes have been received. To prevent overrun, the processor has approximately four byte-reception times (2 milliseconds) to begin reading information out of the FIFO. The processor should continually read the FIFO until bit 1 of the D-Channel Status Register 2 indicates that the FIFO is empty, or bit 0 of the DSR2 indicates that the last byte of the received packet has been read. The processor is then free to perform other functions.

The transmit and receive threshold values are "tunable" variables and depend upon the specific application. For example, experience has shown that threshold values of 4 are the most conservative choices. These values allow the processor a great deal of time to respond to the interrupt while also allowing the processor ample time to perform other tasks between interrupts. A transmit threshold of 4 empty bytes and a receive threshold of 4 bytes is a good starting point for handling the data FIFOs. These values may then be tuned as system performance dictates. When transmitting packets significantly larger than 8 bytes, however, the best system

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performance may be achieved by programming the transmit FIFO threshold with 8 empty bytes and the receive FIFO threshold with 8 bytes. This situation results in a minimum amount of total time spent in the interrupt service routine while maximizing the amount of work done while actually in the interrupt service routine. The trade-off is that the system must be capable of responding to the threshold interrupt quickly enough (375 microseconds for transmit and 425 microseconds for receive) to prevent FIFO overrun and underrun.

DLC INTERRUPTS

Numerous interrupts are associated with the operation of the Data Link Controller (DLC), but not all of them need be enabled in every application. It is normally sufficient to enable interrupts for End of Valid Transmit Packet, End of Receive Packet, Transmit Threshold, Receive Threshold, and any D-Channel Error conditions that are pertinent to the application. This set of interrupts will allow the DSC to monitor all the events that arise during the course of packet data transmission and reception.

End of Receive Packet Interrupt

When an End of Receive Packet (EORP) interrupt occurs, it will appear in the Interrupt Register as a D-Channel Status Register 1 (DSR1) interrupt. An EORP interrupt signifies that a closing flag has been received. Note, however, that the receive FIFO may still contain data from this received packet, and the number of bytes in the FIFO may not be enough to trigger the threshold interrupt. The D-Channel Status Register 2 (DSR2) bit 1 will indicate whether data to be read is still in the Receive FIFO. Any data remaining in the Receive FIFO must be read out 1 byte at a time until DSR2 bit 0 is set, indicating that the last byte of the receive packet has been read. Note that the Last Byte of Receive Packet status goes active *after* the byte has been read.

Reading the last byte of the receive packet causes the D-Channel Error Register (DER) to propagate to the top of the 2-byte DER FIFO, which in turn updates the D-Channel Status Registers and the Interrupt Register. It is important to read DER, DSR1, DSR2, and the Address Status Register (no required order) before reading the D-Channel Receive Byte Count Register (DRCR). Reading the MSB of the DRCR causes the next receive byte count and associated Address Status Register byte to propagate to the output of their respective 2-byte FIFOs, causing the D-Channel Status Registers and Interrupt Register to be updated. At this point, the D-Channel Error Register should be checked to determine if any receive error conditions, such as Overflow or Overrun, exist.

End of Transmit Packet Interrupt

When a packet is to be transmitted, the Transmit FIFO is loaded with a number of bytes, normally 8 for packets larger than 8 bytes. The D-Channel Transmit Byte Count Register (DTCR) is then written, because writing the MSB of the DTCR causes transmission to begin. If the FIFO is not preloaded, the software has to respond very quickly when the DTCR is written to prevent underrun. When the MSB of the DTCR is written, the transmitter will first ensure that it has access to the D channel, and then it will transmit an opening flag. If no data is in the FIFO after the opening flag has been transmitted, an underrun will occur and be followed by a transmit abort. The FIFO then remains reset until the error condition is handled.

The packet transmission will be handled by the interrupt service routine via the Transmit Threshold interrupt until the last byte of the packet has been transmitted. When the closing flag is transmitted, an End of Valid Transmit Packet interrupt will occur to alert the application software that the transmitter is now available for new transmissions. Care must be taken to keep track of how many bytes have been written to the Transmit FIFO, because the D-Channel Transmit Byte Count Register contains the number of bytes that are actually left to be transmitted, including the bytes in the FIFO. This means that software should keep track of how many bytes have been written to the FIFO, and it should stop transferring to the FIFO when the total number of bytes have been written. See the Interrupt Service Routine Transmit FIFO Handler sample code for an example of how this might be handled. After writing this last byte, the processor will exit the interrupt service routine and perform other tasks until it receives the End of Valid Transmit Packet Interrupt. No FIFO cleanup is required when the End of Valid Transmit Packet occurs. The application usually will use this interrupt to inform higher level software that the transmitter is now available to send another packet.

MISCELLANEOUS

Simultaneous Receive Threshold and End of Receive Packet Interrupts

When receiving a packet, it is possible for a Receive Threshold interrupt and an End of Receive Packet interrupt to occur at the same time. For example, if the Receive Threshold was programmed for 4 bytes and the last 4 bytes of a packet are received, the Receive Threshold and the End of Receive Packet interrupts will occur simultaneously. The interrupt service routine will have to handle both of these interrupts. Assuming the Receive Threshold is at a higher priority in the interrupt

service routine than the End of Receive Packet, the Receive Threshold will get serviced first. The receive threshold service routine will be responsible for reading the remaining bytes out of the receive FIFO. After the last byte of the receive packet is read, a flag should be set by the application software indicating all bytes of the current packet have been read. (See the *rcvstatus* software register in the Receive FIFO Handler source code example.) When the End of Receive Packet interrupt is serviced, the rcvstatus software register will be checked to determine if any bytes from the current packet are still in the FIFO. When this flag bit is set in the rcvstatus register, the interrupt service routine knows not to read any more bytes. The Receive Byte Available bit in DSR2 cannot be used for this purpose, because there may be more bytes in the FIFO that belong to the next packet.

Terminated Data Packets

Packet transmission and reception may be terminated in many ways, and this situation must be handled differently depending upon whether transmission or reception was terminated. For example, a packet being transmitted may be intentionally aborted by the application software, or the abort may be the result of an error condition, such as underrun, which terminates the packet transmission. To intentionally abort the transmission, a binary 1 must be written into bit 7 of the Initialization Register. Be sure to write a binary 0 into bit 7 any time after writing the 1, or the Am79C30A will continually issue abort characters and will be unable to begin transmission of the next packet. The transmit data FIFO and all of its internal pointers are reset when a transmit abort occurs. The transmit FIFO will remain in this reset condition until DSR1 and DER are read or the D-Channel Transmit Byte Count Register is written to begin a new transmission.

The case of the receive abort is a bit more complicated because the receive FIFO is capable of holding more than one packet at a time. A perfectly good packet may be in the receive FIFO and then an error condition can occur during reception of the next packet. The erroneous packet reception will be terminated, but the initial packet should remain intact. The current packet reception can be intentionally aborted by writing a binary 1 to bit 6 of the Initialization Register. After 60 microseconds to allow for the abort, a binary 0 must be written into bit 6 or the Am79C30A will continue to abort incoming data. Any time a receive error or intentional abort occurs, the bytes that are already in the receive FIFO will remain there. The only way to remove this data is to read the bytes out one at a time or place the Am79C30A in idle mode. Placing the part in idle mode is normally much too drastic a measure to take, because it essentially halts all functions of the part except LIU activation detection. This means that any voice connection, data transmission, and data reception will be terminated. If it is possible that the bytes in the FIFO are valid data, then the FIFO must be read as normal and the data transferred to local memory for storage. If it is known that *all* the data in the FIFO are garbage, then the data may be read out of the FIFO and discarded until the FIFO is empty. To determine if the FIFO is empty, bit 1 of the D-Channel Status Register 2 (Receive Byte Available) must be monitored until it indicates that no more bytes are available. After reading out the data in the FIFO, the application may have a need for the contents of the status and error registers. Whether or not the status and error registers are read, the DRCR must be read to bring the receive FIFO out of the aborted state. This is normally done anyway when an error condition occurs, so it will not impact performance. The receiver will then go back to searching for an opening flag for the next incoming data packet.

Last Byte Transmitted Interrupt

The Last Byte Transmitted (LBT) status indication is found in the D-Channel Status Register 2 (DSR2) bit 3, and it will generate an interrupt if the D-Channel Mode Register 3 (DMR3) bit 4 is set. The LBT status is generated when the first bit of the last data byte is transmitted out of the transmit FIFO, and its most useful function is to provide the earliest possible indication that the FIFO is available to be loaded with another packet of data. Consider the case of back-to-back packets. As soon as the first bit of the last byte of data is transmitted to the S interface, the LBT status/interrupt will be generated. The remainder of the data byte, the 2-byte FCS, and the closing flag must still be transmitted. In the time it takes for this transmission to take place, the Transmit Byte Count Register can be loaded with the value for the next packet, and the Transmit FIFO can begin being filled with new data. The result of this is that the closing flag for the first packet will be shared as the opening flag of the second packet. This would be the way to maximize the use of the available bandwidth. One very important item to note is that in this mode of operation, an End of Transmit Packet indication will not be generated until the last back-to-back packet transmission is completed.

```
/* If XMT Threshold caused interrupt */
if (intstatreg & TTHRSH) {
  /* While transmit buffer available and all bytes not yet transmitted
  while ((rd_dsc(Dsc->dsr2) & TBA) && RAM->xmtcnt) {
    /* Write a byte from RAM to XMT FIFO */
    wr_dsc(DSC->d_buff, *Ram->xmtnext++);
    /* Decrement transmit byte count */
    Ram->xmtcnt--;
  }
}
```

INTERRUPT SERVICE ROUTINE
TRANSMIT FIFO HANDLER

```
/* If RCV Threshold caused interrupt */
if (intstatreg & RTHRSH) {
  /* Read the d-channel status register */
  dsr2 = rd_dsc(Dsc->dsr2);
  /* While RCV Byte Available in FIFO */
  while (dsr2 & RBA) {
    /* Read a byte from RCV FIFO and place it in local RAM */
    *RAM->rcvfree++ = rd_dsc(Dsc->d_buff);
      /* If last byte of RCV packet then */
      if((dsr2 = rd_dsc(Dsc->dsr2)) & LBRP
      {
        /* Set status flag and break */
        rcvstatus | = RCV_FLAG;
        break;
      }
  }
}
```

INTERRUPT SERVICE ROUTINE
RECEIVE FIFO HANDLER

Link Layer Tutorial

The functions performed by the OSI Data Link Layer (DLL) are described. An overview of the DLL's role in the communication process is presented, as well as a description of the elements that implement the DLL functions. An explanation of the fundamental differences between X.25's LAPB and ISDN's LAPD is included, followed by a brief description of Frame Relay.

DATA LINK LAYER OVERVIEW

The Data Link Layer (DLL) is the second layer in the OSI reference model. It provides services to the Network Layer (Layer 3) and uses the services provided by the Physical Layer (Layer 1). The functions performed by the DLL are independent of the network media (i.e., telephone wires, satellite, coaxial cables, fiber-optic lines, etc.) and deal only with the establishment and maintenance of the communication link connecting source and destination endpoints.

In this application note, the terms "communication link" and "data link" will be used in describing the functions of the DLL. The distinction between the two can best be understood by using the telephone system as an example. In this case, a circuit-switched point-to-point "communication link" is established when the remote party answers the telephone. The "data link" is established when both parties begin exchanging information. Each party can be viewed as a DLL entity implementing a simple protocol for information exchange. Information between the two parties, which may be conveyed in error or is simply unintelligible due to a poor connection, is corrected when one end of the "data link" asks the other end to repeat the information. If the connection is very poor, the "communication link" is terminated by hanging up. Thus, simply stated, the function of the DLL is to ensure the error-free transfer of information across a communication link.

In the telephone example cited, the exchange of information is always point-to-point, even though the routing of the connection may encompass more than one Central Office Exchange or "Hub." In a Packet-Switched Network, however, all Hubs play an equally important role in ensuring the integrity of the data being sent/received. As shown in Figure 1, data sent between source and destination nodes A and B may encompass more than one Hub. The communication links between Hubs are independent of one another, and each Hub incorporates a DLL entity in the form of a protocol that establishes the rules for proper data exchange.

The information that determines which path is taken through the network, and hence the total number of communication links and data link entities involved, is embedded within defined bit fields of each data packet being transferred. It is the responsibility of the DLL to ensure that this "Network Layer" information and user data are transferred without error, and in proper sequence, from its source Hub (point A) to its destination Hub (point B). Each Hub along the path stores the packets and verifies their integrity before forwarding them to the next Hub. From this point of view, the DLL and the Network Layer can be thought of as always operating on a point-to-point basis, but with the Network Layer having the additional capability of routing data from an incoming point-to-point data link to an outgoing point-to-point data link.

In the case where the destination node B resides on a multi-drop or multipoint link (Figure 2), Data Link 3 can be thought of as implementing individual point-to-point data links that are multiplexed over the same physical channel. In cases such as these where the multipoint network is not geographically dispersed, the Network Layer is defined as being null (not implemented) since routing occurs at a higher layer.

Examples of DLL protocols are Bisynchronous (BISYNC) and Synchronous Data Link Control (SDLC) of IBM's SNA, Digital Data Communications Message Protocol (DDCMP) of DEC's DECNET, Ethernet's Local Area Network (LAN) IEEE 802 standard, and ISO's High-level Data Link Control (HDLC), a subset of which is known as LAPB (Link Access Procedure Balance), and is the accepted DLL protocol of CCITT's X.25 packet switch specification. Both BISYNC and DDCMP are referred to as Character-Oriented Protocols (COP), and HDLC and SDLC are referred to as Bit-Oriented Protocols (BOP). The fundamental difference between the two is in the way Layer 3 data is enveloped before it is released to the physical layer. The material presented in this appplication note deals solely with the specifics of HDLC/SDLC.

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The following sections define the structures used and functions performed by the DLL in more detail.

THE DATA LINK LAYER

Much like the partitioning found in the IEEE 802 LAN standard (IEEE 802 standard partitions its DLL into two sublayers: the Logical Link Control [LLC] and the Media Access Control [MAC] sublayers), the OSI's DLL can also be viewed as consisting of two sublayers: the "frame" sublayer and the "sequence" sublayer. The frame sublayer deals with frame delineation, data transparency, and physical layer error detection; whereas the sequence sublayer deals with commands and responses (the actual protocol) that are used in ensuring that the information arrives error free and in proper sequence over the communication link. The frame sublayer (sometimes referred to as Layer 2–) is specified in ISO-3309 High-level Data Link-Frame Structure, and the sequence layer (sometimes referred to as Layer 2+) is specified in ISO-4335 High-level Data Link-Elements of Procedures.

THE SEQUENCE SUBLAYER

Two modes in the ISO-4335 document determine how the sequence layer is applied over the communication link. These two modes are: the Normal Response Mode (NRM) which is a procedure based on a master-slave principle using two types of stations, primary and secondary, with different functional capabilities, and the Asynchronous Balance Mode (ABM) which is a procedure based on combined stations (stations with both master and slave capability).

In NRM operation the primary station is responsible for data link connection, disconnection, and error recovery. Secondary stations only respond to commands from the primary and, in general, are not allowed to transmit unless given permission to do so from the primary station. This mode of operation is commonly used in half-duplex and multipoint data links, and is the mode of operation most commonly found in IBM SNA environments. IBM's SDLC implements a subset of the HDLC Elements of Procedures and can be found in IBM document GA27-3093-3.

In ABM operation each station is responsible for data link connection, disconnection, and error recovery, and either station can transmit without permission from the other station. ABM stations always operate on a point-to-point basis and never multipoint. This HDLC mode of operation is the "sequence" sublayer specified in CCITT's X.25 DLL specification, and is referred to as Link Access Procedure Balanced (LAPB).

Embedded within the control field of every Layer 2 frame is a Poll (P)/Final (F) bit which is used by the sequence sublayer in maintaining the data link. This bit is used to solicit responses from another station. Its use, however, differs when operating in NRM or ABM (LAPB). In NRM a command frame from the primary station with the P bit set causes the secondary station to initiate transmission. A response frame from the secondary station with the F bit set indicates the final frame of transmission. Data transmission in NRM is always half duplex. In LAPB, however, a command frame from one combined station with the P bit set solicits a response frame from the remote station with the F bit set, but data transmission occurs at full duplex. In both NRM and ABM, timers are started when a frame with the P bit set is sent, and error recovery procedures are instigated if a timeout occurs before a frame with the F bit set is received.

THE FRAME SUBLAYER

The frame sublayer deals with the frame structure used to transport Layer 3 data over the physical layer. It deals with frame delineation, the method used in achieving data transparency, and the algorithm (CRC) used for error detection over the physical layer.

Frame delineation is performed in both SDLC and HDLC by the use of an 8-bit flag character (01111110) that indicates the start and the end of a Layer 2 frame and determines the location of the address field, control field, and the first bit of the information field. The closing flag determines the location of the 16-bit Frame Check Sequence (FCS). In order to preclude the occurrence of flag characters between the opening and closing flags of a frame, all information between them is subjected to a 0-bit insertion/deletion algorithm where the transmitter inserts a 0 bit immediately following the occurrence of 5 consecutive 1 bits. The receiver then does the opposite by deleting any 0 bit that occurs after 5 consecutive 1 bits.

The address field is used for identifying source and destination endpoints on the data link, and for the proper interpretation of command or response frames. In LAPB, for example, the address field of a command frame transmitted to a remote station contains the address of the remote station, whereas the address field of a response frame transmitted from the remote station contains the address of that station.

The control field conveys the functional operation of the data link in the form of commands and responses between Hubs. Examples of commands and responses (covered in ISO-4335) are Receiver Ready (RR), Receiver Not Ready (RNR), Set Asynchronous Balance Mode (SABM), and Disconnect (DISC) for commands and RR, RNR, and Disconnected Mode (DM) for responses. Thus, it is through the control field that the sequence sublayer protocol is implemented.

The Frame Check Sequence (FCS) is a 16-bit CRC character inserted between the end of the information field and the closing flag of a frame, used to ensure data integrity over the physical layer. This 16-bit character is

calculated based on the data sent using a specific algorithm. The receiver uses the same algorithm to calculate the CRC character on the received data and compares the result with the 16-bit CRC character received. A mismatch results in an error and the frame is discarded without alerting the next higher layer. The discarding of the frame eventually results in its retransmission by the sequence sublayer. The algorithm used to generate the 16-bit CRC character is based on the CCITT standard polynomial $X^{16}+X^{12}+X^5+1$.

HDLC FRAMES

Three types of HDLC frame formats (Figures 3a and 3b) are used for transporting data over the physical layer: (1) Information frames (I frames), (2) Supervisory frames (S frames), and (3) Unnumbered or Unacknowledged frames (U frames). In addition, an Extended or Non-Extended frame format can be specified.

I frames are used to transport data and are sequentially numbered with send (Ns) and receive (Nr) sequence numbers. The address, control, and FCS fields are the only fields acted on by the DLL entity, while an acknowledged information field is always passed on to the next higher layer (Layer 3). In HDLC, the length of the information field can be any number of bits, whereas IBM's SDLC restricts the length to an integer number of bytes. The maximum information field transmitted in either case, however, is application dependent.

S frames are used to acknowledge correctly received I frames, to request retransmission in case of errors, and to implement flow control (that is, request a temporary suspension of the transmission of I frames).

U frames are used for data link initiation or disconnection, reporting procedural errors, and for transferring data which is not sequenced.

The extended or non-extended frame format refers to the modulus of the sequence numbers, N(s) and N(r), used. Sequence numbers of I frames cycle through a set of numbers 0, 1, 2, ..., M-1, where M is the modulus number. The extended control field uses a modulus number of 128 and the non-extended control field format uses a modulus number of 8. The extended mode is used in cases where long propagation delays are involved, because a station must stop transmitting I frames if it has M-1 unacknowledged I frames outstanding. An implication of the extended mode is that more memory is required because each Hub stores all transmitted I frames, and they are not passed on to the next layer until they have been successfully acknowledged by the corresponding peer sequence sublayer. The selection of Extended/Non-Extended frame format in LAPB, for example, is done via the Set Asynchronous Balance Mode Extended (SABME) or the Set Asynchronous Balance Mode (SABM) U-frame command.

ISDN

The intent of the Integrated Services Digital Network (ISDN) is to integrate a set of services (voice and data) over standard telephone cabling. In order to accomplish this, two types of channels have been defined within the scope of the ISDN; a B channel and a D channel. A B channel refers to one of two full-duplex 64-kb/s channels used to transport digitized voice or data through the network. A D channel refers to a single full-duplex 16-kb/s channel that is shared among two or more users over the physical layer interface, and is used for transporting B-channel signaling and low-speed data. Because this scheme involves communication over a point-to-multipoint link, a new DLL protocol referred to as Link Access Procedure D channel (LAPD) was developed.

Link Access Procedure D (LAPD) is covered in CCITT's I.441 (Q.921). LAPD Layer 2 frames, used to transport data over the D channel, are based on the HDLC framing, with Layer 3 based on CCITT's Q.931. Hence, much of what has already been presented with regard to the DLL (frame sublayer and sequence sublayer) applies directly to LAPD.

The LAPD frame format is shown in Figures 4a and 4b. A major difference in an LAPD frame is that the address field is defined to be 2 bytes instead of 1 as in LAPB, and is more fully utilized. Since LAPB is always point-to-point, its address field is used only to distinguish between command and response frames, whereas in LAPD, the address field is used to distinguish between other Layer 2 entities. The LAPD Command/Response (C/R) bit, however, is used in a similar way that the LAPB address field is used in differentiating command from response frames.

The LAPD address field consists of two subfields: a DLL Service Access Point Identifier (SAPI) used to indicate which protocol entity is to receive the Layer 2 frame, and a Terminal Endpoint Identifier (TEI) used for distinguishing between the various terminals connected on a data link. For example, according to CCITT I.441, a SAPI field received with a value of 0 identifies the *Layer 2 frame* as having call control information for the specified TEI, and a SAPI field received with a value of 16 identifies the Layer 2 frame as having packet information for the specified TEI.

Thus, the most significant functional difference between LAPB and LAPD is that LAPD provides logical channel multiplexing at the data link layer (LAPD supports point-to-multipoint physical layer connections with "logical" channel multiplexing at the data link layer), whereas LAPB provides this same capability at the Network Layer (LAPB supports only point-to-point at the physical and data link layers with logical channel multiplexing oc-

curring at the Network Layer via Logical Channel Number [LCN] assignment).

FRAME RELAY

X.25 data link layer protocol software design is typically based on the use of state event tables that help implement a finite state machine. Using this technique, the software is designed such that it is always in a specific state at any instant in time. These table-driven state machines define all the states that the protocol can be in at any instant in time, plus all the events that can occur while in a specific state, what actions need to occur because of events, and what new state will be entered into as a result of the event occurring. In short, the current state and event information are used to index into a two-dimensional structure to determine what the next state will be. This translates to the use of a rather large case statement since the software must search the table each time an event occurs. With LAPD's multiplexing capability at the data link layer, intermediate Hubs can perform their internetwork switching tasks without having to process the complete DLL protocol, thus minimizing the massive state table searches.

This has prompted the CCITT in adopting a new mode of packet switch service referred to as Frame Relay. What Frame Relay does is combine the LAPD, SAPI, and TEI fields into a single field that is used in much the same way that LCNs are used in X.25's network layer. Each intermediate Frame Relay Hub only examines the first two fields of an LAPD frame when routing a frame, and only detects misaddressed or errored frames (frame CRC bad). Thus, the need for massive state tables is minimized and improvements in throughput are possible since much of the Layer 2 and 3's protocol overhead has been removed and made the responsibility of the communicating endpoints.

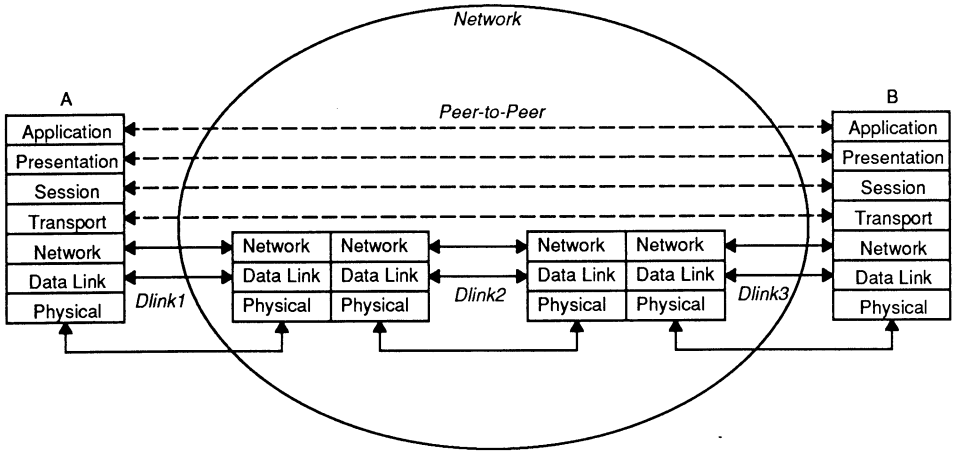

Figure 1

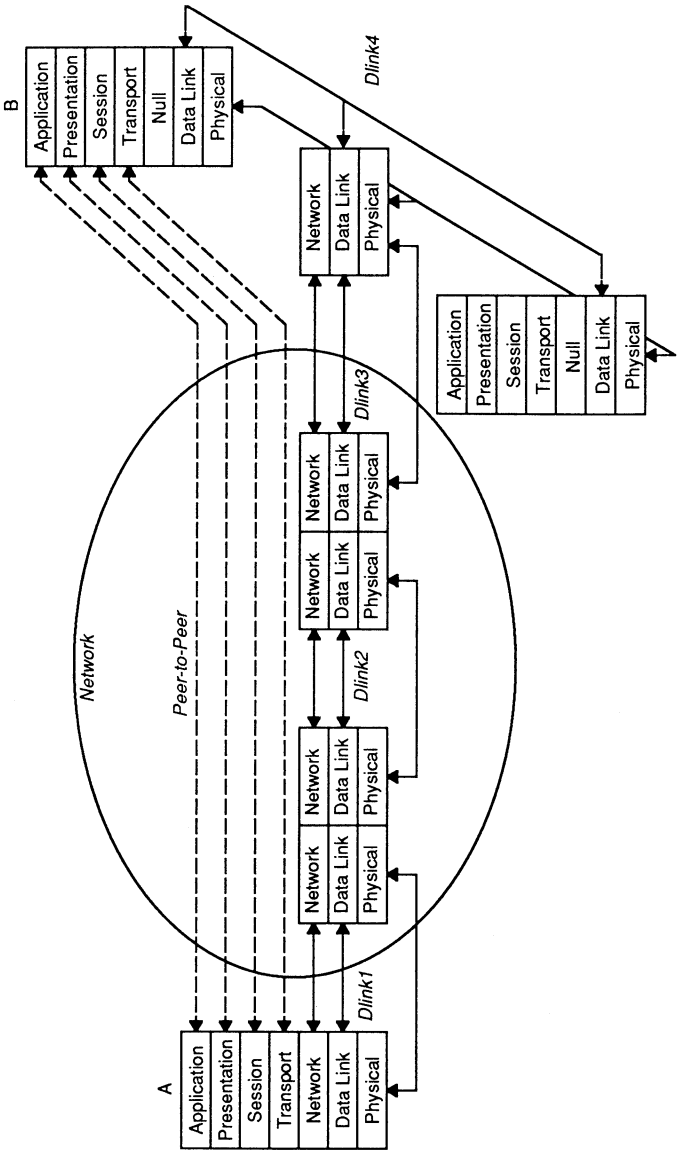
B
Application
Presentation
Session
Transport
Null
Data Link
Physical
Dlink4
Network
Data Link
Physical
Application
Presentation
Session
Transport
Null
Data Link
Physical
Network
Peer-to-Peer
Dlink3
Dlink2
Dlink1
A
Application
Presentation
Session
Transport
Network
Data Link
Physical

Figure 2

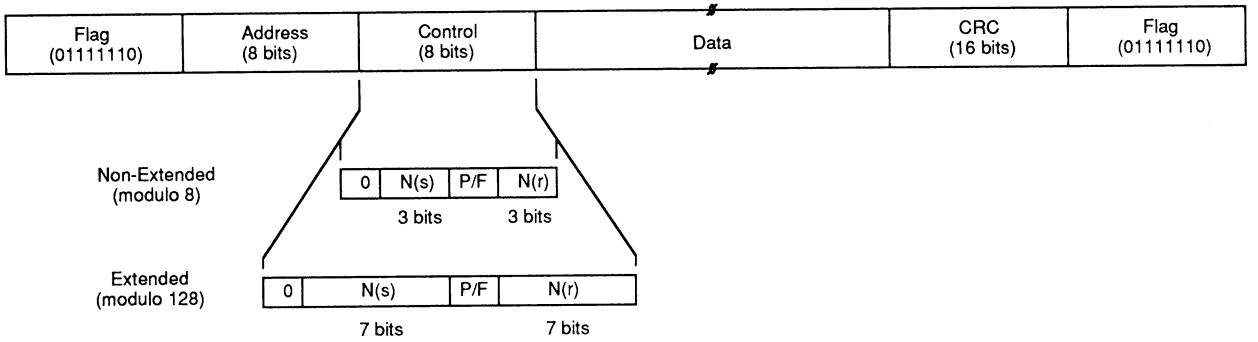

Figure 3a. I Frame

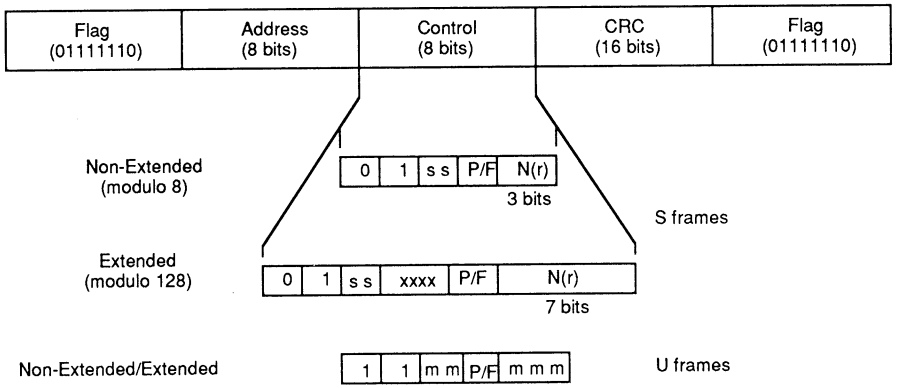

Figure 3b. U and S Frames

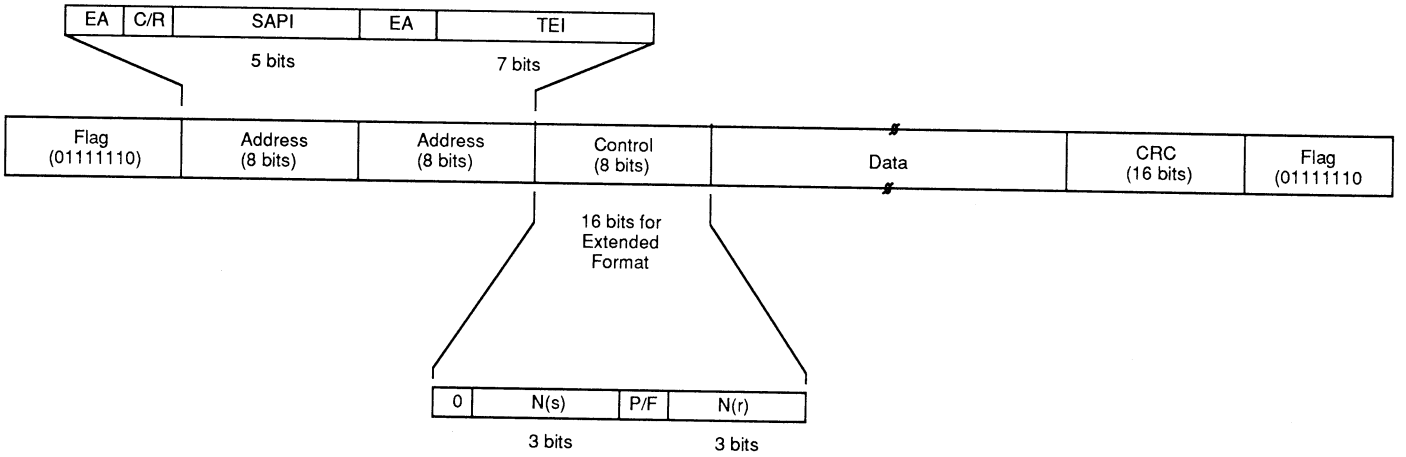

Figure 4a. LAPD I Frames

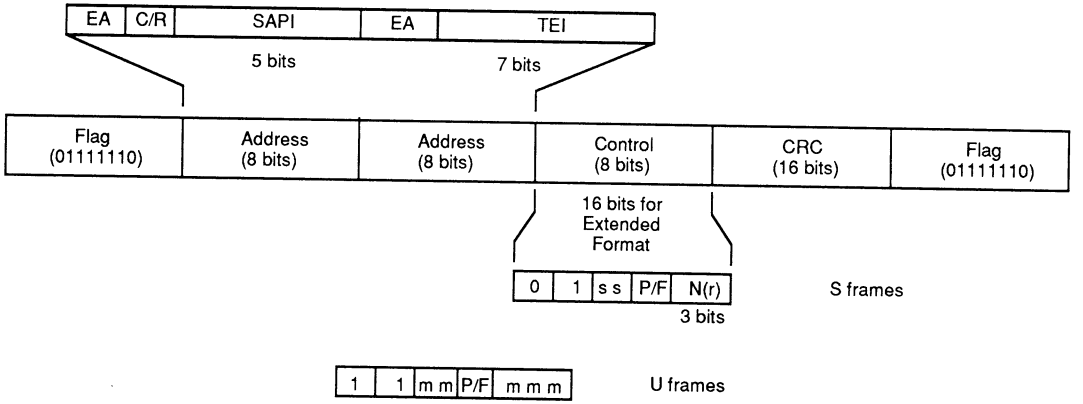

Figure 4b. LAPD S and U Frames

Am79C30A Oscillator Considerations

Care is required in the selection of oscillator components for microprocessors and peripherals to avoid problems in oscillator startup, stability, and accuracy. This selection process is especially critical in a communications application such an ISDN transceiver, where even a small frequency error can measurably degrade S interface performance.

INTRODUCTION

In many microprocessor and peripheral applications, the absolute frequency and stability (over temperature, power supply, and unit-to-unit variation) of the clock source is not critical; it is often sufficient that the oscillator starts reliably and runs at a nominally accurate frequency. In an ISDN S interface transceiver application, however, the frequency accuracy is critical due to CCITT specifications for jitter and timing. Unexpected results may also arise when interfacing the DSC to commercial audio transmission test equipment. Some of these test sets do not operate as true clock slaves, but instead use internal phase lock loops to synchronize to the device under test. If the device clock is even slightly out of specification, synchronization failure or artificially low transmission performance measurements may result.

OSCILLATOR ALTERNATIVES

The designer has three basic options for clocking the DSC: using an external packaged oscillator, constructing an external crystal-based oscillator, or connecting load capacitors and a crystal to the XTAL1 and XTAL2 pins.

Use of an external packaged oscillator presents the minimum number of complications to the designer and is the most expensive solution of the three. The oscillator output is simply connected to the XTAL2 input, and the XTAL1 output is left unconnected. The frequency accuracy, supply tolerance, and stability of the oscillator is specified by its manufacturer, thus the designer does not need to be concerned with discrete component selection. In this case, the designer needs to verify that the oscillator frequency is guaranteed to be 12.288 MHz ±80 ppm in the expected operating environment, and that the oscillator output is electrically compatible with the DSC datasheet requirements for the XTAL2 input. The first point to note is that the XTAL2 input levels are not TTL-compatible; V_{IH} must be at least 0.8 V_{CC}, while V_{IL} must be less than 0.8 volts. This is important to note since packaged oscillators are available with a variety of output characteristics, including CMOS and TTL. In the event that the source oscillator provides TTL levels, a CMOS buffer with TTL-compatible input levels may be used to provide the correct levels to the DSC. It is important to note that adding a pullup resistor to a TTL-output device is absolutely *not* an acceptable method of creating higher levels for clock inputs on CMOS or NMOS devices. On the Low to High transition, the output driver will only actively drive to typically 3.4 V, after which the output voltage will rise exponentially with a time constant dependent on the pullup resistor and parasitic characteristics of the driver and load. The rise time, duty cycle, and jitter of the resulting clock may be unacceptable and will vary greatly with temperature, device, and power supply level and noise.

Constructing an external crystal-based oscillator is an alternative when designing with the DSC, but presents design complexities without offering any compensating benefits. Use of the DSC on-chip oscillator is much simpler than an external design, and the MCLK output is available if it is desired to clock other devices. It is recommended not to attempt to drive other devices by connecting a buffer to the XTAL1 output; the extra load is an additional variable that may negatively impact oscillator performance.

Use of the on-chip oscillator is the most cost-effective approach, and will yield excellent results as long as precautions in component selection and placement are observed. To understand the problems that may be encountered, it is beneficial to review some basic properties of quartz crystals.

QUARTZ CRYSTAL PROPERTIES

Quartz is a piezoelectric material, meaning that an internal E field will form in response to applied mechanical stress. Conversely, application of an external voltage will cause mechanical deformation. It follows that if a quartz sample is driven with an AC voltage, it will cause the crystal to mechanically vibrate. The reactance of the quartz crystal does not vary monotonically with frequency, but instead becomes positive over ranges of frequency that correspond to the natural vibrational modes of the crystal. The fundamental idea behind the

design of a crystal oscillator circuit is to force the crystal to oscillate at or near a preselected natural frequency of vibration.

The lowest natural frequency of vibration is called the fundamental mode, and is illustrated in Figure 1. There are usually higher modes of vibration, called mechanical overtones, which are not necessarily frequency harmonics of the fundamental mode. In addition, there may be numerous "parasitic" responses where the reactance becomes positive over a narrow frequency range. Generally, crystals are intended to be operated in their fundamental mode, but it is possible to realize oscillation at a selected overtone by using a combination of careful oscillator design and crystal manufacture.

CRYSTAL RESONATOR MANUFACTURE

Manufacture of a crystal resonator begins with the slicing of a crystal wafer from a larger crystal. It is important to note that many key crystal properties are highly dependent on the "cut" of the wafer (that is, the relation between the sample faces and the crystal axes). For instance, the favorability of the various vibrational modes depend greatly upon the cut of the quartz employed. The variation of frequency with respect to temperature is also dependent upon the cut. Thus, the selection of cut is made based upon the intended application of the crystal.

After rough shaping, the crystal is planed in order to coarsely set the frequency. The thinner a wafer of quartz is, the higher the frequency of oscillation will be. Fundamental mode crystals are limited to approximately 40 MHz, since at higher frequencies the wafers become too thin to withstand mechanical vibration. For higher frequencies, crystals are cut to favor an overtone mode of vibration.

After planing, the wafer is fitted with electrodes and a holder. It is common at this point to make the final adjustment of frequency by placing the crystal assembly into a test oscillator circuit and carefully plating the crystal with silver or aluminum. The addition of mass reduces the frequency of vibration, and is continued until the desired frequency is achieved. The assembly is hermetically sealed after plating, and is referred to as a crystal resonator.

For low applied voltages the crystal deformation is elastic, but application of an excessive voltage will result in mechanical deformation beyond the elastic limit of the crystal and it will shatter. The power dissipation in a crystal is specified as its Drive Level, but this parameter is not significant in a semiconductor application.

QUARTZ CRYSTAL CIRCUIT MODEL

For the purpose of circuit analysis, it is convenient to represent a quartz crystal by the equivalent circuit illustrated in Figure 2. The series RLC components are often referred to as the motional parameters, while C_0 represents the capacitance of the electrodes and holder. The series resistance does not play a very significant role in oscillation, as long as the circuit used to drive the crystal has sufficient gain. In general, series resistance should be as low as possible. The crystal equivalent model is said to be in series resonance when L_1 and C_1 are in resonance, that is:

$$F_S = (2 \cdot pi)^{(-1)} \cdot (L_1 \cdot C_1)^{(-1/2)} \qquad \text{eq. 1}$$

This equation assumes that C_0 may be neglected. At frequency F_S the reactance of the crystal equivalent circuit is zero, as illustrated in Figure 1. It is possible to construct circuits in which a crystal will appear purely resistive and oscillate at its series resonance frequency. However, in semiconductor applications, it is not common practice to operate a crystal at series resonance.

THE PARALLEL RESONANT OSCILLATOR

Figure 3 illustrates a typical "parallel" resonant oscillator circuit, where the crystal is used in conjunction with two load capacitors C_{ld} (assumed to be equal for simplicity) and a parasitic capacitance C_{par}, which represents trace

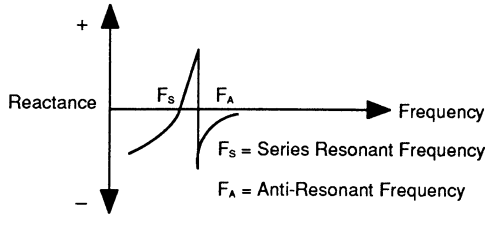

Figure 1. Crystal Reactance versus Frequency

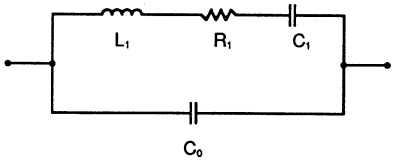

Figure 2. Crystal Equivalent Circuit

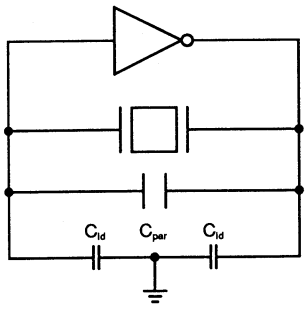

Figure 3. Parallel Resonant Oscillator

and pin capacitance, along with imperfections of the amplifier. It is easily seen that the three capacitors may be represented by a single parallel capacitance:

$$C_L = (1/2) \cdot C_{ld} + C_{par} \qquad \text{eq. 2}$$

The circuit shown in Figure 3 will oscillate at the frequency where the (negative) reactance of C_L is cancelled by the (positive) reactance of the crystal. From Figure 1, it is apparent that the reactance of the crystal in the fundamental mode is positive between frequencies F_S and F_A. Thus, depending upon the load capacitor value C_{ld} and the parasitic capacitance C_{par}, the circuit in Figure 3 will oscillate at a frequency somewhere between F_S and F_A. For many applications the precise frequency of oscillation is not critical, but for applications such as communications it may be necessary to control the frequency more tightly.

CALCULATION OF FREQUENCY VARIATION

The fact that oscillation frequency varies with load capacitance is of great significance in both crystal specification and oscillator component selection. In terms of specification, it is necessary to understand how crystals are calibrated. There is no such thing as a parallel-resonant crystal; the term refers to the method of calibration. When a crystal specification states, for instance, that a crystal is "12.288 MHz, ±0.05%, parallel resonant, 20 pF," it means that the frequency was calibrated to within 0.05% in the presence of a 20-pF series capacitance. It does *not* mean that the crystal requires 20-pF load capacitors! The value of capacitance required depends upon the amplifier circuit, and to a lesser degree upon the board layout. The following equation describes the relationship between frequency deviation (F_d) from the series resonance point and the crystal circuit parameters:

$$F_d = (F_S \cdot C_0) / [2 \cdot r \cdot (C_0 + C_L)] \qquad \text{eq. 3}$$

where $r = C_0/C_1$, and C_L is the total added load capacitance. Note that this equation indicates that not all crystals will respond identically to a change in load capacitance. Let us now apply Equations 1 through 3 to the following actual crystal parameters to illustrate how the various parameters affect oscillator operation:

$F_S = 12.283823$ MHz

$C_0 = 4.25$ pF

$R_1 = 7.7$ ohms

$C_1 = 0.0165746$ pF

$L_1 = 10.128$ mH

12.288 MHz, ± 20 ppm

Parallel resonant, 20.12 pF

Plugging the above values into Equation 3 yields a frequency offset F_d of 4177 Hz. It is easily verified that this corresponds to the difference between 12.288 MHz and 12.283823 MHz. Now suppose we would like to determine the tolerance of capacitance required to ensure 80-ppm frequency accuracy. Since the crystal frequency is calibrated to within 20 ppm, we will specify the tolerance of the external components to allow for an operating range of ±60 ppm. This corresponds to an operating range as follows:

$$12.28726 \text{ MHz} < f < 12.28874 \text{ MHz}$$

The lower limit corresponds to a frequency offset of 3440 Hz from the series resonance point, while the upper limit corresponds to an offset of 4920 Hz. Plugging F_d = 3440 Hz into Equation 3 yields a C_L value of 25.34 pF, while F_d = 4920 yields a C_L value of 16.44 pF. Note that increasing the load capacitance decreases the operating frequency. The 60-ppm frequency accuracy requirement can be met over the range:

$$16.44 \text{ pF} < C_L < 25.34 \text{ pF} \qquad \text{eq. 4}$$

The parasitic capacitance C_{par} of Equation 2 is on the order of 5–8 pF, and can be determined empirically by changing load capacitors and applying the foregoing equations. It is important to note that the value C_{par} will vary slightly from one device to another, thus not all of the error tolerance should be allotted to the load capacitors. Assuming an empirically determined C_{par} of average value 5 pF, selecting load capacitors of value 30 pF and 5% tolerance allows C_{par} to vary between approximately 2.19 and 9.59 pF, which provides an adequate margin.

RECOMMENDATIONS

It is apparent in Equation 2 that the equivalent load seen by a crystal depends upon both the load capacitors and the parasitic capacitances present. For this reason, it is desirable to minimize the variability of parasitic capacitance by placing both the crystal and the load capacitors as close as possible to the IC oscillator pins. This technique has the added benefits of minimizing the capacitive coupling of other signals into the oscillator, and reducing the amount of clock noise coupled into other circuits. It is also preferable to operate with larger load capacitances, since the percentage contribution of both load capacitor error and parasitic capacitance is reduced. If the load capacitor value becomes too large, however, oscillator startup problems may ensue. For power-critical applications, it should be noted that increasing load capacitance will result in increased power consumption.

Although the equations are useful to gain insight into the problem, there is no substitute for actual measurement. It is recommended to select a load capacitor value for a given crystal by lab measurement of the DSC MCLK output frequency (so as not to load the oscillator circuit), and then using the manufacturer's parameter values in the foregoing equations as a check. This procedure need only be done during initial design; it does not need to be repeated on a per-unit basis. It is also recommended to select load capacitors with minimum temperature variation, for instance, ceramic NPO capacitors.

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Design of Crystal and Other Harmonic Oscillators, Benjamin Parzen, John Wiley and Sons.

Introduction to Quartz Crystal Unit Design, Virgil E. Bottom, Van Nostrand Reinhold.

Designing Quartz Crystals into Integrated Circuits and Microprocessors, John B. Fisher, Standard Crystal Corporation Application Note.

The author would like to gratefully acknowledge many helpful inputs from the applications staff of Saronix Corporation, Palo Alto, California.

Electret Handset Interface

The electret-type microphone, incorporating a capacitive microphone and built-in FET, is rapidly becoming the microphone of choice for telephone applications. A bias circuit is required for the FET, along with a gain stage for pre-amplification of the low output voltage.

THE ELECTRET HANDSET

The electret handset is a popular choice among telephone designers for a variety of reasons. It is inexpensive, light, and requires less bias current than the conventional carbon-type microphone. Furthermore, the microphone provides excellent dynamic range and noise performance, and its small physical size makes it suitable for many different handset designs.

The electret microphone provides an output voltage when pressure from the speaker's voice varies the charge on an internal capacitor, which in turn varies the gate voltage of a FET. Since a drain current must exist for the FET amplifier, the electret microphone requires an external bias resistor.

The microphone satisfies part of its gain requirement with the FET amplifier, but requires an additional gain stage to boost the signal up to a level compatible with the Am79C30A MAP receiver. It should be noted that the bias and gain requirements will vary from one handset manufacturer to another, and may require some adjustment for compliance with any applicable sound pressure level tests. For the handset tested, a gain of approximately 24 dB was selected to provide a subjectively comfortable listening level.

BIAS AND GAIN CIRCUITRY

The circuit shown in the attached figure was designed with several objectives. First, it was designed to operate using only a 5-V power supply. Second, it was essential that the circuit would perform adequately with an inexpensive operational amplifier. Finally, it was necessary that the circuit would provide satisfactory performance in a noisy environment, for instance, on a personal computer board.

In Figure 1, the equivalent circuit for the electret microphone shows a variable capacitor driving a FET. The series combination of the 6.8-kohm and 3.3-kohm resistors provides approximately 0.5 mA of bias current for the FET. The 6.8-kohm resistor and the 20-microfarad capacitor serve to filter noise from the 5-V power supply, since any power supply noise would otherwise appear at the microphone output and be inseparable from the voice signal. This is especially critical since the noise would be boosted by 24 dB through the amplifier.

The operational amplifier is a typical inverting configuration, with the positive input biased to approximately 2.4 volts by the DSC AREF signal. The 10-kohm and 1-μF capacitor to ground form an RC filter to remove any low-level switching noise from the AREF signal, because this noise could be objectionable after being boosted by the amplifier. The 560-pF capacitor in the amplifier feedback path removes high frequencies from the signal path, thereby ensuring that they are not converted to in-band noise by operational amplifier imperfections. The value of this feedback capacitor may need to be varied for different models of op-amps.

The 1-μF capacitor on the output of the amplifier is necessary to AC couple the signal to the analog input of the DSC. The 15-kohm resistor ensures that the analog input is biased with the voltage provided by the DSC AREF pin. The analog input must be biased by the AREF voltage, otherwise degraded transmission performance at low signal levels will occur.

TEST RESULTS AND RECOMMENDATIONS

The described circuit was built and tested using low-cost TLC271CP and TL061ACP operational amplifiers manufactured by Texas Instruments. A Wandel and Goltermann PCM4 test set was used to perform Signal to Distortion, Gain Tracking, Idle Channel Noise, Relative Group Delay, and Absolute Gain measurements in accordance with CCITT Recommendation G.714. All tests were passed with satisfactory margins using the aforementioned op-amps on a four-layer PCB installed in an IBM PC-AT.

In designing audio interfaces for the Am79C30A DSC, it is important to note that the weakest link in the audio path is the circuitry external to the DSC. Care must be taken to ensure that microphone bias current is adequately filtered. Board layout is also critical to optimize audio performance. Audio traces should be as short as possible, and routed away from high-speed digital signals such as clocks. Splitting the ground and V_{CC} planes

of the PCB is an effective technique and is described in a companion application note on DSC Layout Hints. The ground points of the various analog components of the microphone circuit should be placed as close as possible to one another on the board in order to minimize the effect of different ground current return paths.

In prototyping analog circuitry, it must be understood that wirewrap boards and high-gain audio amplifiers do not mix very well. Long wires, crosstalk, insufficient power supply decoupling, stray inductances and capacitances, and poor grounding all contribute to a higher noise floor and degraded amplifier stability.

As a final precaution, note that care must be taken in op-amp selection. The amplifier must be capable of running on 0- and 5-V power supplies and must have sufficient voltage swing around the nominal 2.4-V AREF voltage to handle the maximum expected audio signal without distortion.

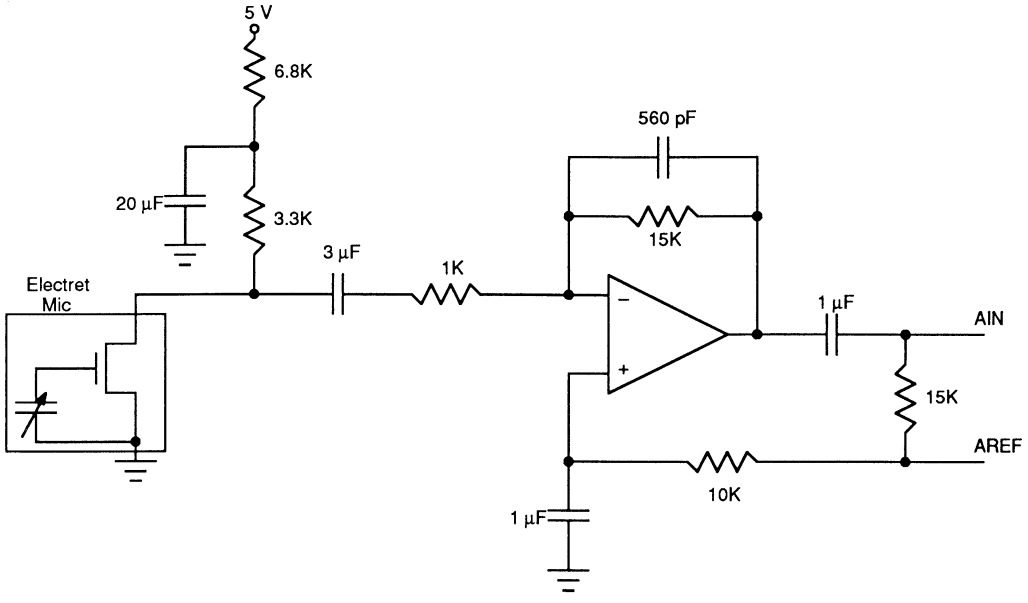

Figure 1. Electret Handset Interface

Protocol Reference Model Tutorial

The introduction of the Open System Interconnect (OSI) model for networks has had a profound effect on data communications and distributed applications processing. The acceptance of this standard continues to widen as the OSI model was selected as the basic structure for the software-intensive ISDN. It is important for engineers working in this area to be familiar with the basic terminology and concepts of the OSI reference model and the developing ISDN reference model.

The data communications industry in the early 1970s was characterized by incompatibility between product offerings from different vendors. Although some of these differences were due to a lack of applicable standards, manufacturers were also reluctant to share design information because they wanted to protect their customer bases. As the size of the market grew, it became increasingly apparent that it was in everyone's best interest to provide the capability to interconnect equipment from different manufacturers. In 1978, the International Standards Organization (ISO) began work on developing the "Open System Interconnect" reference model to provide a framework for the orderly communication of "application processes" across different computer networks. These application processes may be human users or computer programs. The committee considered input from a variety of international trade and standards organizations and produced a working standard within three years. The work of this committee was also supported by the CCITT in their recommendation X.200.

The framework chosen by the ISO is a seven-layer structure in which each layer provides specialized services that logically belong together. There are, of course, many different ways in which the functions may be organized, and the standard acknowledges that it would be difficult to provide the optimality of any given approach. In order to achieve agreement, the committee was also required to take note of existing solutions and standards. A brief description of each layer, its purpose, and services provided follows.

The Physical Layer is the lowest layer of the architecture and, as defined in CCITT X.200, "provides mechanical, electrical, functional, and procedural means to activate, maintain, and deactivate physical connections for bit transmission between data link entities." For instance, the physical layer may include functions such as connector types and pinouts, line code definitions, clocking and timing requirements, voltage levels, block formats, activation and deactivation procedures, loopback modes, and error notification. A good example of a physical layer protocol is RS-449. In the ISDN environment, a key physical layer protocol is CCITT I.430, which describes the four-wire S or T interface.

The Data Link Layer resides directly above the physical layer and provides for the transfer of units of information between the two ends of the physical link, as well as the establishment and release of the data link connection. Framing, flow control, error detection, and error correction are possible functions to include in this layer. Multiplexing, another key feature of this level, provides multiple logical connections on a single physical link. HDLC and SDLC are examples of common Layer 2 protocols. In the ISDN application, CCITT Q.921 (LAPD) is the key Layer 2 protocol for data link signaling on the D channel.

The Network Layer is the third layer of the architecture and is responsible for the addressing, switching, and routing functions that are required to guarantee transparent transmission of data through a system of computers. It is important to note that a network may not always be sourcing or sinking data, but may be performing a relay function as illustrated in Figure 13/X.200. The switching of data through an ISDN is an example of a relay function. The network must guarantee transparency of such a relay function to higher protocol layers. In the ISDN application at Layer 3, CCITT Q.931 provides call setup and teardown functions. However, in the special case of "nailed-up" D-channel data service, there is no routing to be done, and only X.25 is required at Layer 3.

The Transport Layer is responsible for providing the required performance at minimum cost based upon the current state of the network, and is the lowest layer that is concerned with end-to-end functions. As seen in Figure 13/X.200, no transport layer service is required for the intermediate system in a relay network.

The Session Layer coordinates the interaction of the application processes at each end regarding session establishment, release, management, and error reporting. There is no flow control at the session layer.

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The Presentation Layer provides for the conversion of data between different representations, for instance, code, character, or format conversions.

The Application Layer provides all the services directly required by the application process, since it is the only layer in the model that communicates directly to the application processes. Services will vary greatly depending upon the application, including, for example, identification of an intended communication partner by name or address, or determination of the availability of the requested party.

One of the objectives in the definition of the OSI layers was to simplify the amount of communication required between layers. Each layer, except the application layer, is defined to provide services to the next higher OSI layer. Adjacent layers interact with predetermined requests and responses, called primitives. Note that the OSI model does not attempt to define primitives, but leaves this to the individual protocols used in specific applications. At each layer there is a "peer protocol" to govern the interaction between entities in the layer, as illustrated in Figure 12/X.200.

Entities within a layer can communicate only through the services provided by the next lower layer, and it is assumed that physical layer entities interact directly.

In spite of the detailed description of the functions in each layer, it is important to note that the OSI model does not constrain the implementation architecture; the definition of system management functions is left completely to the user. The CCITT is working on a series of recommendations for Management Entities, but they are a long way from completion and are far more complex than the OSI model itself.

Figure 13/X.200 illustrates communication through a relay system that passes data between two systems that are only connected through the intermediate network. An ISDN may be viewed as such a relay system, but with the possibility of ongoing participation even after a call is established. In recent years the CCITT has been developing Recommendation I.320, the objective of which is to model the interconnection and exchange of user information and control information in an ISDN environment. In this sense, I.320 may be viewed as a specific application of the principles of X.200 and not as a radically different recommendation. Although I.320 is still evolving, it is useful to examine the emerging ISDN Protocol Reference Model. In the February 1988 draft of I.320, it is stated that "the support of outband signaling, the ability to activate supplementary services during the active phase of the call, imply a separation between control information and user information." To reflect this separation, I.320 introduces the concept of a control plane (C plane) and user plane (U plane). Both of these planes have seven layers in the manner of the OSI model, but not all layers are necessarily present. The purpose of the U plane is the transfer of information among user applications, whereas the C plane is intended to establish or modify a network connection or to provide supplementary services. The C and U planes do not connect directly, but instead communicate via primitives through the plane management function M, which is not layered (at this time). This basic reference model is illustrated in Figure 2/I.320, which is reproduced from the 1985 version of I.320. In the February 1988 draft of I.320, the model was further refined to split the C plane into local and global control planes. This alteration was made to reflect the fact that control data handled by an entity may concern an adjacent (local) entity or non-adjacent (remote or global) entity. The resultant Generic Protocol Block is illustrated in Figure 3/I.320, but it must be emphasized that I.320 is not finalized and thus is subject to considerable change.

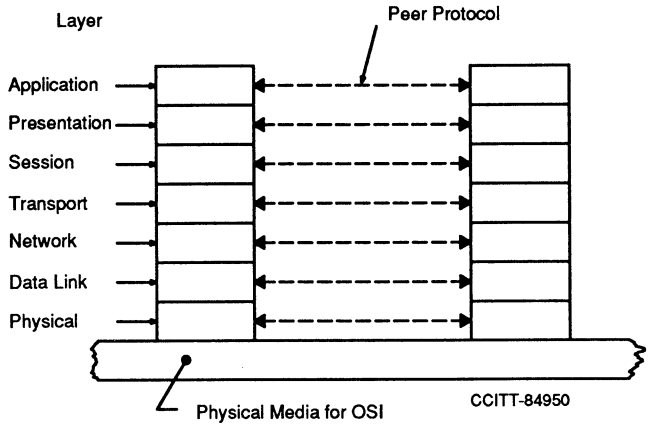


Figure 12/X.200. Seven-Layer Reference Model and Peer Protocols

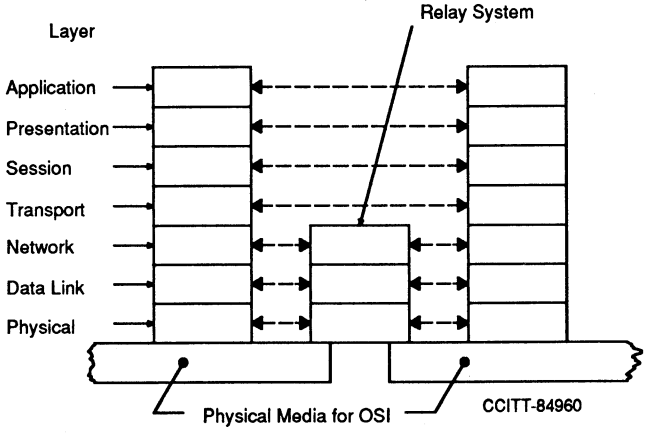
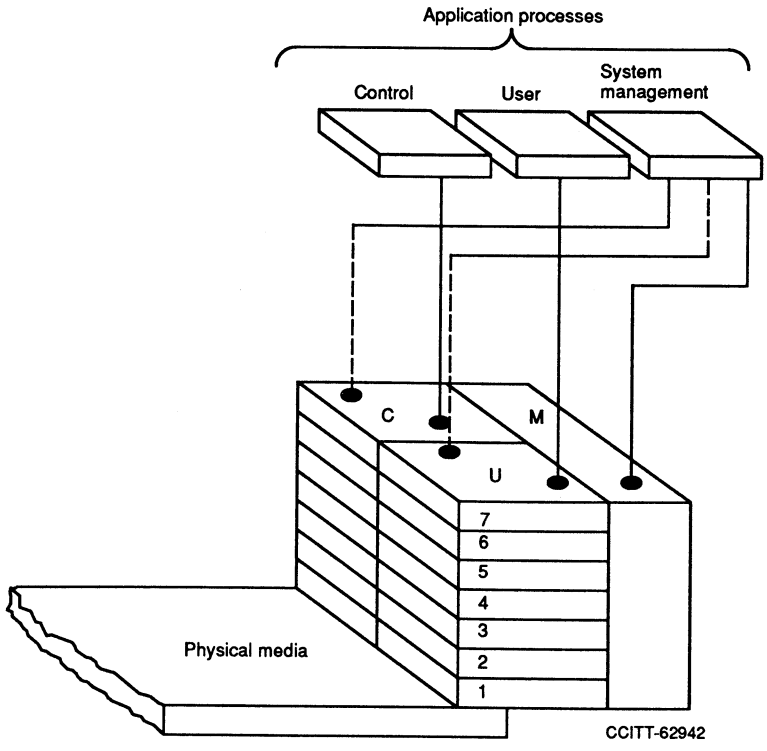


Figure 13/X.200. Communication Involving Relay Open Systems



Note: Peer-to-peer protocols associated with U and C are not shown.

Figure 2/I.320. Interactions Associated with a Protocol Block

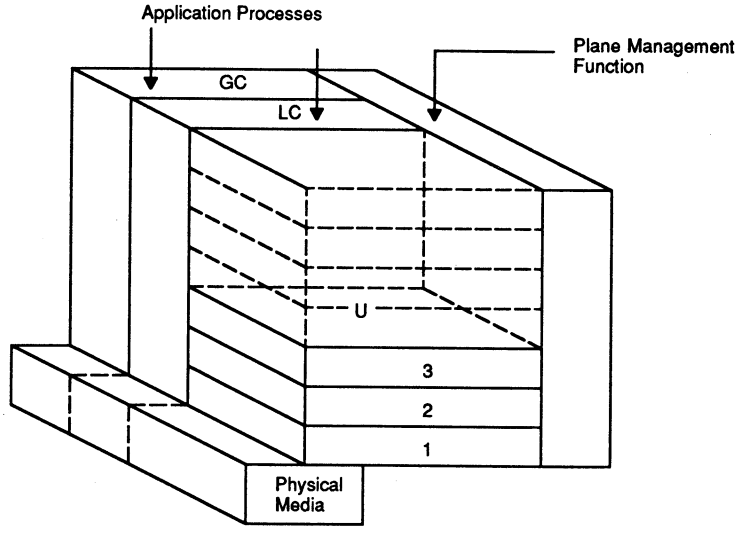


Figure 3/I.320. Generic Protocol Block

RECOMMENDED FOR FURTHER READING

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Telecommunication Technology, R.L. Brewester, John Wiley & Sons, 1986.

Telecommunications Networks, Protocols, Modeling, and Analysis, Mischa Schwartz, Addison-Wesley, 1987.

CCITT Recommendation X.200: "Reference Model of Open Systems Interconnection for CCITT Applications."

CCITT Recommendation X.210: "Open System Interconnection Layer Service Definition Conventions."

CCITT Draft Recommendation I.320: "ISDN Protocol Reference Model."

Key Design Hints for the DSC/IDC

Due to the high level of integration of the Am79C30A/32A DSC/IDC, it is easy to overlook important design information when reading the data sheet. The following list of key design hints has been compiled to streamline the design process. A comprehensive series of ISDN application notes and tutorials is available from Advanced Micro Devices; please contact an AMD sales office or factory for current information.

1. The AREF pin *must* be used to bias the AINA and AINB inputs. There is a data sheet parameter Vios that states that the analog inputs must be biased to within 5 mV of AREF. AREF is *nominally* 2.4 volts; normal device-to-device variation will exceed the 5-mV Vios specification. If a voltage other than AREF is used, transmission performance at low signal levels will be degraded.
2. The recommended method of biasing the AINA or AINB inputs is to use a 15–100 kohm resistor between the input and AREF. The signal source should be AC-coupled to the analog input. Care should be taken such that the RC formed by the biasing resistor and blocking capacitor does not distort the input signal. A 3-dB point below 10 Hz is recommended.
3. The AREF output must not be loaded with a capacitor, since it may cause the internal buffer amplifier to become unstable. For some applications involving significant gain external to the DSC, the AREF output may require a simple RC noise filter. In this case, the AREF output should be isolated from the capacitor by a resistance of greater than 1 kohm to ensure stability.
4. The DSC/IDC should be provided with decoupling capacitors, situated as closely as possible to the package power leads. In general, 0.1-µF ceramic capacitors are sufficient, but bulk decoupling capacitors will be required if the LS1 and LS2 loudspeaker outputs are driving a heavy load.
5. The DSC/IDC is constructed on a single substrate, and therefore the device power pins must not be from separate supplies. If there is a DC offset between the analog and digital power supply pins, excessive current may flow through the device substrate.
6. The LS1, LS2, and EAR1, 2 outputs are intended to be used differentially. Although it is possible to use only a single output, the rejection of power supply noise and internal digital noise is improved if the outputs are used differentially.
7. It is necessary to observe the maximum loading specification for the LS and EAR outputs. When used differentially, the EAR outputs must see a minimum of 540 ohms between them. Similarly, the LS outputs must see a minimum of 40 ohms. The maximum capacitive loading in either case is 100 pF.
8. The LS and EAR outputs do not need to be "matched" to the load. The LS and EAR outputs are voltage drivers and do not assume the presence of any particular load impedance. As long as the maximum loading specification is met, the LS and EAR outputs will function satisfactorily. In some cases an external resistor may be used to center the desired output volume, for instance, while driving a 150-ohm earpiece with the EAR outputs.
9. For Revision D and prior releases, it is not recommended to unnecessarily access the ATGR, FTGR, GX, GR, GER, STG, X, R, MMR1, and MMR2 registers while audio is active. When the microprocessor accesses these registers, it may interfere with the MAP calculations, resulting in degraded transmission performance or audible noise.
10. When using programmable gains and filters in the MAP, it is necessary to consider dynamic range effects such as truncation error and clipping. In case of questions in any particular application, please contact AMD applications staff for assistance.
11. All MAP tone generators are referenced with respect to the +3-dBm0 overload voltage, that is, a 0-dB tone yields a +3-dBm0 output. Care must be taken to avoid clipping when adding tones to signals as, for example, when generating DTMF waveforms.
12. The RC connected to CAP1/CAP2 must be situated as close as possible to the DSC package to reduce the amount of noise coupled in from other signal traces.

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13. It is necessary to observe the XTAL2 frequency accuracy requirement of 12.288 MHz, ±80 ppm. Since crystals from different manufacturers will vary, it is necessary to measure the DSC oscillator output frequency at the MCLK pin and, if necessary, adjust the value of the crystal load capacitors as part of the initial design procedure. An application note of oscillator considerations is available from AMD.
14. If driving the XTAL2 pin with an external oscillator, it is necessary to observe the data sheet input voltage and rise/fall time requirements. Note that the XTAL2 levels are not TTL-compatible.
15. The DSC, as any sensitive analog device, requires care in board layout. An application note of DSC board layout hints is available from AMD.
16. The sidetone path defaults to −18 dB attenuation. If it is desired to disable the sidetone path, it is necessary to enable the sidetone block and program it for infinite attenuation.
17. The LIU transformers, series resistors, and IC LIU output drivers must be considered as a functional unit. Transformers that meet CCITT I.430 requirements with other transceivers are not necessarily appropriate for use with the DSC, and vice versa. An application note of DSC transformer and series resistor considerations is available from AMD.
18. Interrupts should be masked when reading or writing any indirect or multi-byte DSC registers, to prevent the possibility of an interrupt occurring and destroying the contents of the Command Register.

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